(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
6 October 2005 (06.10.2005)

PCT

(10) International Publication Number
WO 2005/093831 A1

(51) International Patent Classification[7]: H01L 23/49

(21) International Application Number:
PCT/US2005/004459

(22) International Filing Date: 14 February 2005 (14.02.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/544,800 13 February 2004 (13.02.2004) US
60/579,967 15 June 2004 (15.06.2004) US

(71) Applicant *(for all designated States except US)*: **PRESIDENT AND FELLOWS OF HARVARD COLLEGE** [US/US]; 17 Quincy Street, Cambridge, MA 02138 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **LIEBER, Charles, M.** [US/US]; 27 Hayes Avenue, Lexington, MA 02173 (US). **WU, Yue** [CN/US]; 27 Lee Street, #3, Cambridge, MA 02139 (US). **XIANG, Jie** [CN/US]; 88 Beacon Street, Apt. 16, Somerville, MA 02143 (US). **YANG, Chen** [CN/US]; 20 Peabody Terrace, Apt. 32, Cambridge, MA 02138 (US). **LU, Wei** [CN/US]; 35 Concord Avenue, #1, Cambridge, MA 02138 (US).

(74) Agent: **OYER, Timothy, J.**; Wolf, Greenfield & Sacks, P.C., 600 Atlantic Avenue, Boston, MA 02210 (US).

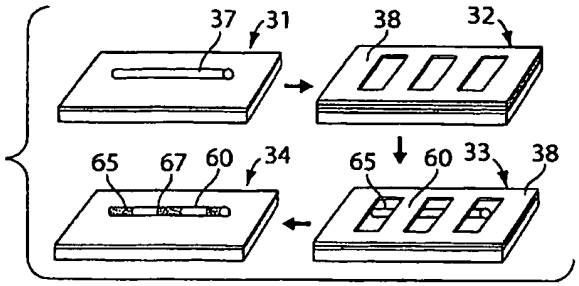
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: NANOSTRUCTURES CONTAINING METAL-SEMICONDUCTOR COMPOUNDS



(57) Abstract: The present invention generally relates to devices and components for use in nanotechnology and sub-microelectronic circuitry that include metal-semiconductor compounds such as metal silicides. The present invention also, in some embodiments, provides methods of forming such devices and components by allowing a first material to diffuse into a second material, optionally creating a new compound. Thus, as an example, metal atoms are allowed to diffuse into a semiconductor to create the metal-semiconductor compound. In some cases, the device may include a component that is a single crystal. Certain metal-semiconductor compounds of the invention have novel physical/electrical properties, for example, low resistivities, high conductivities, high current density capacities, and the like. In some embodiments, a component of the invention may have two or more regions that differ in composition, where one or both of the regions can include a metal-semiconductor compound. In some cases, the regions may be created by using a mask or a nanoscale wire to define the two or more regions.

WO 2005/093831 A1

NANOSTRUCTURES CONTAINING METAL-SEMICONDUCTOR COMPOUNDS

FEDERALLY SPONSORED RESEARCH

The present invention was sponsored by DARPA, Grant No. N-00014-01-1-0651. The U.S. Government may have certain rights to the present invention.

FIELD OF INVENTION

The present invention relates generally to nanotechnology and sub-microelectronic circuitry, as well as associated methods and devices. In particular, the present invention relates to components for use in nanotechnology and sub-microelectronic circuitry that include metal-semiconductor compounds such as metal silicides. Articles and devices of size greater than the nanoscale are also included.

DISCUSSION OF RELATED ART

Interest in nanotechnology, in particular sub-microelectronic technologies such as semiconductor quantum dots and nanowires, has been motivated by the challenges of chemistry and physics at the nanoscale, and by the prospect of utilizing these structures in electronic, optical, and other related devices. Nanoscopic articles may be well-suited for transport of charge carriers and excitons (e.g. electrons, electron hole pairs, etc.) and thus may be useful as building blocks in nanoscale electronics, optics, and other applications.

SUMMARY OF INVENTION

The present invention generally relates to components for use in nanotechnology and sub-microelectronic circuitry that include metal-semiconductor compounds such as metal silicides. Most aspects and embodiments of the present invention involve nanometer-scale articles and devices, but larger articles and devices are provided as well. The subject matter of the present invention involves, in some cases, interrelated products, one or more solutions to a particular problem, and/or a plurality of different uses of one or more systems and/or articles.

In one aspect, the present invention is a method. In one set of embodiments, the method includes providing a bulk metal adjacent a semiconductor wire, and diffusing at least a portion of the bulk metal into at least a portion of the semiconductor wire and thereby changing that portion from a semiconductor to a conductor, where the

semiconductor wire comprises at least one portion having a smallest dimension of less than about 500 nm. The method, in another set of embodiments, includes diffusing a material into at least a portion of a wire, where the wire comprises at least one portion having a smallest dimension of less than about 500 nm.

The method, according to another set of embodiments, includes an act of diffusing a metal into at least a portion of a semiconductor nanoscale wire to form a stoichiometric ratio of metal atoms to semiconductor atoms within the portion of the semiconductor nanoscale wire. In yet another set of embodiments, the method includes an act of bulk-doping at least a portion of a nanoscale wire after growth of the nanoscale wire. The method, in still another set of embodiments, includes an act of diffusing a material into a center portion of a semiconductor wire. In some cases, the semiconductor wire comprises at least one portion having a smallest dimension of less than about 500 nm. In one embodiment, the method includes an act of converting a conductor into a semiconductor. In another embodiment, the method includes an act of converting a semiconductor into a conductor.

The present invention includes an article in another aspect. In one set of embodiments, the article includes a wire or other nanostructure. In one embodiment, the wire or nanostructure comprises at least one metal silicide, where the wire or other nanostructure is a single crystal. In another embodiment, the wire or other nanostructure includes a compound having a stoichiometric ratio of silicon and at least one metal. In some cases, the wire or other nanostructure has at least one portion having a smallest dimension of less than about 500 nm. The wire or other nanostructure, in another embodiment, comprises at least one metal silicide having a resistivity of less than about 60 microOhm cm. In some cases, the wire or other nanostructure may have resistivity of less than about 60 microOhm cm. In yet another embodiment, the wire or other nanostructure includes at least one metal silicide able to carry a current density of at least about 10^8 A/cm^2. In certain instances, the wire or other nanostructure is able to carry a current density of at least about 10^8 A/cm^2.

In another embodiment, the wire or other nanostructure comprises at least two regions differing in composition, where at least one region comprising a metal silicide, and where the wire or other nanostructure comprises at least one portion having a smallest dimension of less than about 500 nm. In still another embodiment, the wire or other nanostructure includes at least two regions that differ in composition and a

boundary between the regions, where the boundary has a maximum dimension of less than about 500 nm and at least one region comprises a metal silicide.

In another aspect, the present invention is directed to a method of making one or more of the embodiments described herein, for example, a nanoscale wire comprising a metal silicide. In yet another aspect, the present invention is directed to a method of using one or more of the embodiments described herein. In still another aspect, the present invention is directed to a method of promoting one or more of the embodiments described herein.

Other advantages and novel features of the present invention will become apparent from the following detailed description of various non-limiting embodiments of the invention when considered in conjunction with the accompanying figures. In cases where the present specification and a document incorporated by reference include conflicting and/or inconsistent disclosure, the present specification shall control.

BRIEF DESCRIPTION OF DRAWINGS

Non-limiting embodiments of the present invention will be described by way of example with reference to the accompanying figures, which are schematic and are not intended to be drawn to scale. In the figures, each identical or nearly identical component illustrated is typically represented by a single numeral. For the purposes of clarity, not every component is labeled in every figure, nor is every component of each embodiment of the invention shown where illustration is not necessary to allow those of ordinary skill in the art to understand the invention. In the figures:

Fig. 1A is a schematic diagram of a technique used to prepare a nanowire comprising a metal-semiconductor compound, in accordance with one embodiment of the invention;

Figs. 1B-1D are photomicrographs of various nanowires comprising metal-semiconductor compounds;

Figs. 2A-2B illustrate graphs of current versus voltage for certain nanowires of the invention

Fig. 3A is a schematic diagram of a method of making a nanowire that includes at least one heterojunction, according to an embodiment of the invention;

Figs. 3B-3D are photomicrographs of certain nanowires of the invention having heterojunctions, where each nanowire includes at least one region that comprises a metal-semiconductor compound;

Fig. 4A is a graph of current versus voltage for a nanowire including a heterojunction, where at least one region of the nanowire comprises a metal-semiconductor compound, in accordance with one embodiment of the invention;

Figs. 4B-4D illustrate various nanowires that include heterojunctions, useful as transistors;

Figs. 5A-5C are schematic diagrams illustrating one embodiment of the invention;

Figs. 6A-6F illustrate other methods of making a nanowire that includes at least one heterojunction, according to another embodiment of the invention; and

Figs. 7A-7G illustrate certain silicide nanowires of the invention, and their performance characteristics.

DETAILED DESCRIPTION

The present invention generally relates to devices and components for use in nanotechnology and sub-microelectronic circuitry that include metal-semiconductor compounds such as metal silicides. The present invention also, in some embodiments, provides methods of forming such devices and components by allowing a first material to diffuse into a second material, optionally creating a new compound. Thus, as an example, metal atoms are allowed to diffuse into a semiconductor to create the metal-semiconductor compound. In some cases, the device may include a component that is a single crystal. Certain metal-semiconductor compounds of the invention have novel physical/electrical properties, for example, low resistivities, high conductivities, high current density capacities, and the like. In some embodiments, a component of the invention may have two or more regions that differ in composition, where one or both of the regions can include a metal-semiconductor compound. In some cases, the regions may be created by using a mask or a nanoscale wire to define the two or more regions.

The indefinite articles "a" and "an," as used herein in the specification and in the claims, unless clearly indicated to the contrary, should be understood to mean "at least one." As used herein, "or" should be understood to mean inclusively or, i.e., the inclusion of at least one, but including more than one, of a number or list of elements. Only terms clearly indicated to the contrary, such as "only one of" or "exactly one of," will refer to the inclusion of exactly one element of a number or list of elements. The term "plurality," as used herein, means two or more. A "set" of items may include one or more of such items.

The term "fluid" generally refers to a substance that tends to flow and to conform to the outline of its container. Typically, fluids are materials that are unable to withstand a static shear stress. When a shear stress is applied to a fluid, it experiences a continuing and permanent distortion. Typical fluids include liquids and gasses, but may also include free-flowing solid particles, viscoelastic fluids, and the like.

Certain devices of the invention may include wires or other components of scale commensurate with nanometer-scale wires, which includes nanotubes and nanowires. In some embodiments, however, the invention comprises articles that may be greater than nanometer size (e. g., micrometer-sized). As used herein, "nanoscopic-scale," "nanoscopic," "nanometer-scale," "nanoscale," the "nano-" prefix (for example, as in "nanostructured"), and the like generally refers to elements or articles having widths or diameters of less than about 1 micron, and less than about 100 nm in some cases. In all embodiments, specified widths can be a smallest width (i.e. a width as specified where, at that location, the article can have a larger width in a different dimension), or a largest width (i.e. where, at that location, the article has a width that is no wider than as specified, but can have a length that is greater).

As used herein, a "wire" generally refers to any material having a conductivity of any semiconductor or any metal, and in some embodiments may be used to connect two electronic components such that they are in electronic communication with each other. For example, the term "electrically conductive" or a "conductor" or an "electrical conductor" when used with reference to a "conducting" wire or a nanoscale wire, refers to the ability of that wire to pass charge. In certain instances, the electrically conductive material can have a resistivity lower than about 10^5 microOhm cm ($\mu\Omega$ cm), lower than about 10^4 microOhm cm, lower than about 10^3 microOhm cm, lower than about 100 microOhm cm, or lower than about 10 microOhm cm.

A "nanoscopic wire" (also known herein as a "nanoscopic-scale wire" or "nanoscale wire") generally is a wire, that at any point along its length, has at least one cross-sectional dimension and, in some embodiments, two orthogonal cross-sectional dimensions less than 1 micron, less than about 500 nm, less than about 200 nm, less than about 150 nm, less than about 100 nm, less than about 70, less than about 50 nm, less than about 20 nm, less than about 10 nm, or less than about 5 nm. In other embodiments, the cross-sectional dimension can be less than 2 nm or 1 nm. In one set of embodiments, the nanoscale wire has at least one cross-sectional dimension ranging from 0.5 nm to 200

nm. Where nanoscale wires are described having, for example, a core and an outer region, the above dimensions generally relate to those of the core. The cross-section of a nanoscopic wire may be of any arbitrary shape, including, but not limited to, circular, square, rectangular, annular, polygonal, or elliptical, and may be a regular or an irregular shape. The nanoscale wire may be solid or hollow. Any nanoscale wire can be used in any of the embodiments described herein, including carbon nanotubes, nanorods, nanowires, nanowhiskers, organic or inorganic conductive or semiconducting polymers, and the like, unless otherwise specified. Other conductive or semiconducting elements that may not be molecular wires, but are of various small nanoscopic-scale dimensions, can also be used in some instances, e.g. inorganic structures such as main group and metal atom-based wire-like silicon, transition metal-containing wires, gallium arsenide, gallium nitride, indium phosphide, germanium, cadmium selenide, etc. A wide variety of these and other nanoscale wires can be grown on and/or applied to surfaces in patterns useful for electronic devices in a manner similar to techniques described herein involving nanoscale wires, without undue experimentation. The nanoscale wires, in some cases, may be formed having dimensions of at least about 1 micron, at least about 3 microns, at least about 5 microns, or at least about 10 microns or about 20 microns in length, and can be less than about 100 nm, less than about 75 nm, less than about 50 nm, or less than about 25 nm in thickness (height and width). The nanoscale wires may have an aspect ratio (length to thickness) of greater than about 2:1, greater than about 3:1, greater than about 5:1, greater than about 10:1, greater than about 25:1, greater than about 50:1, greater than about 75:1, greater than about 100:1, greater than about 150:1, greater than about 250:1, greater than about 500:1, greater than about 750:1, or greater than about 1000:1 or more in some cases.

A "nanowire" (e. g. comprising silicon and/or another semiconductor material, for example, a metal-semiconductor compound such as NiSi) is a nanoscopic wire that is generally a solid wire, and may be elongated in some cases. Preferably, a nanowire (which is abbreviated herein as "NW") is an elongated semiconductor, i.e., a nanoscale semiconductor. A "non-nanotube nanowire" is any nanowire that is not a nanotube. In one set of embodiments of the invention, a non-nanotube nanowire having an unmodified surface is used in any arrangement of the invention described herein in which a nanowire or nanotube can be used.

As used herein, a "nanotube" (e.g. a carbon nanotube) is generally nanoscopic wire that is hollow, or that has a hollowed-out core, including those nanotubes known to those of ordinary skill in the art. "Nanotube" is abbreviated herein as "NT." Nanotubes are used as one example of small wires for use in the invention and, in certain embodiments, devices of the invention include wires of scale commensurate with nanotubes.

As used herein, an "elongated" article (e.g. a semiconductor or a section thereof) is an article for which, at any point along the longitudinal axis of the article, the ratio of the length of the article to the largest width at that point is greater than 2:1.

As used herein, a "width" of an article is the distance of a straight line from a point on a perimeter of the article, through the center of the article, to another point on the perimeter of the article. As used herein, a "width" or a "cross-sectional dimension" at a point along a longitudinal axis of an article is the distance along a straight line that passes through the center of a cross-section of the article at that point and connects two points on the perimeter of the cross-section. The "cross-section" at a point along the longitudinal axis of an article is a plane at that point that crosses the article and is orthogonal to the longitudinal axis of the article. The "longitudinal axis" of an article is the axis along the largest dimension of the article. Similarly, a "longitudinal section" of an article is a portion of the article along the longitudinal axis of the article that can have any length greater than zero and less than or equal to the length of the article. Additionally, the "length" of an elongated article is a distance along the longitudinal axis from end to end of the article.

As used herein, a "cylindrical" article is an article having an exterior shaped like a cylinder, but does not define or reflect any properties regarding the interior of the article. In other words, a cylindrical article may have a solid interior, may have a hollowed-out interior, etc. Generally, a cross-section of a cylindrical article appears to be circular or approximately circular, but other cross-sectional shapes are also possible, such as a hexagonal shape. The cross-section may have any arbitrary shape, including, but not limited to, square, rectangular, or elliptical. Regular and irregular shapes are also included.

As used herein, an "array" of articles (e.g., nanoscopic wires) comprises a plurality of the articles, for example, a series of aligned nanoscale wires, which may or may not be in contact with each other. As used herein, a "crossed array" or a "crossbar

array" is an array where at least one of the articles contacts either another of the articles or a signal node (e.g., an electrode).

Many nanoscopic wires as used in accordance with the present invention are individual nanoscopic wires. As used herein, "individual nanoscopic wire" means a nanoscopic wire free of contact with another nanoscopic wire (but not excluding contact of a type that may be desired between individual nanoscopic wires, e.g., as in a crossbar array). For example, an "individual" or a "free-standing" article may, at some point in its life, not be attached to another article, for example, with another nanoscopic wire, or the free-standing article may be in solution. This is in contrast to nanotubes produced primarily by laser vaporization techniques that produce materials formed as ropes having diameters of about 2 nm to about 50 nm or more and containing many individual nanotubes (see, for example, Thess, *et al.*, "Crystalline Ropes of Metallic Carbon Nanotubes," *Science*, 273:483-486 (1996), incorporated herein by reference in its entirety for all purposes). This is also in contrast to conductive portions of articles which differ from surrounding material only by having been altered chemically or physically, *in situ*, i.e., where a portion of a uniform article is made different from its surroundings by selective doping, etching, etc. An "individual" or a "free-standing" article is one that can be (but need not be) removed from the location where it is made, as an individual article, and transported to a different location and combined with different components to make a functional device such as those described herein and those that would be contemplated by those of ordinary skill in the art upon reading this disclosure.

In some embodiments, at least a portion of a nanoscopic wire may be a bulk-doped semiconductor. As used herein, a "bulk-doped" article (e. g. an article, or a section or region of an article) is an article for which a dopant is incorporated substantially throughout the crystalline lattice of the article, as opposed to an article in which a dopant is only incorporated in particular regions of the crystal lattice at the atomic scale, for example, only on the surface or exterior. For example, some articles such as carbon nanotubes are typically doped after the base material is grown, and thus the dopant only extends a finite distance from the surface or exterior into the interior of the crystalline lattice. It should be understood that "bulk-doped" does not define or reflect a concentration or amount of doping in a semiconductor, nor does it necessarily indicate that the doping is uniform. In particular, in some embodiments, a bulk-doped semiconductor may comprise two or more bulk-doped regions. Thus, as used herein to

describe nanoscopic wires, "doped" refers to bulk-doped nanoscopic wires, and, accordingly, a "doped nanoscopic (or nanoscale) wire" is a bulk-doped nanoscopic wire. "Heavily doped" and "lightly doped" are terms the meanings of which are clearly understood by those of ordinary skill in the art.

The present invention, in one aspect, includes a nanoscopic wire or other nanostructured material comprising a metal-semiconductor compound. The nanoscopic wire may be, for example, a nanorod, a nanowire, a nanowhisker, or a nanotube. The nanoscopic wire may be used in a device, for example, as a semiconductor component, a pathway, etc. In some cases, the nanoscopic wire may further include, in addition to the metal-semiconductor compound, materials such as semiconductors, dopants, etc.

As used herein, a "metal-semiconductor compound" is a compound that includes at least one metal combined with a semiconductor. In metal-semiconductor compounds of the invention, at least one portion of the compound includes a metal and a semiconductor present in a stoichiometrically defined ratio, i.e., the metal atoms and the semiconductor atoms are present within the compound (i.e., on the atomic scale) in a whole number ratio that is chemically defined, i.e., defined on the basis of the atomic interactions between the metal atoms and the semiconductor atoms within the compound that lead to a ratio of elements present dictated by the bonding principles of chemistry (e.g. coordination chemistry, atomic and molecular orbital interactions and formation, crystal packing, and/or the like). This is to be distinguished from alloys or mixtures, which are simply blends of two or more atoms in a substance, in which the atoms can be mixed together in any ratio, where the ratio is not determined by stoichiometric interactions between the atoms, and doping, where, e.g., ion bombardment of a material with a dopant leads to non-stoichiometric amounts of the dopant in the host material dictated by the amount of dopant introduced. Instead, the metal atoms and the semiconductor atoms in a metal-semiconductor compound interact on the atomic level in a defined fashion, thus resulting in the metal-semiconductor compound having a whole number ratio between the metal atoms and the semiconductor atoms within the compound, i.e., the ratio is dictated by atomic interactions between the metal atoms and the semiconductor atoms within the compound. Thus, the stoichiometric ratio between the metal atoms and the semiconductor atoms is always the same on the atomic level (i.e., at any location within the compound). As an example, there may be ionic charged interactions between the metal atoms and the semiconductor atoms such that, for charge

neutrality, there is a stoichiometric ratio between the metal atoms and the semiconductor atoms within the compound, for example, MZ, M_2Z, M_2Z_3, MZ_2, M_3Z_2, or the like, where M is a metal and Z is a semiconductor. A specific non-limiting example is nickel silicide, NiSi. In some cases, more than one type of metal atom and/or more than one type of semiconductor atom may be present in the metal-semiconductor compound. It should be recognized, of course, that measurements of the ratio of two or more atoms in a compound are not necessarily always exact, due to experimental error and other practical limitations. Thus, in some cases, the ratio so measured may be stoichiometric in reality, even though the experimental measurements deviate somewhat from whole number ratios. As an example, the actual ratios determined for a metal-semiconductor compound may be within about 10% or about 5% of a stoichiometric, whole number ratio.

In one set of embodiments, the metal within the metal-semiconductor compound is a transition metal, for example, an element from one or more of Group IB, Group IIB, Group IIIB, Group IVB, Group VB, Group VIB, Group VIIB, or Group VIIIB. In some cases, Group VIIIB metals may be particularly useful within the metal-semiconductor compound, for example, nickel, iron, palladium, platinum, iridium, etc.

As used herein, the term "Group," with reference to the Periodic Table, is given its usual definition as understood by one of ordinary skill in the art. For instance, the Group II elements include Mg and Ca, as well as the Group II transition elements, such as Zn, Cd, and Hg. Similarly, the Group III elements include B, Al, Ga, In and Tl; the Group IV elements include C, Si, Ge, Sn, and Pb; the Group V elements include N, P, As, Sb and Bi; and the Group VI elements include O, S, Se, Te and Po. Combinations involving more than one element from each Group are also possible. For example, a Group II-VI material may include at least one element from Group II and at least one element from Group VI, for example, ZnS, ZnSe, ZnSSe, ZnCdS, CdS, or CdSe. Similarly, a Group III-V material may include at least one element from Group III and at least one element from Group V, for example GaAs, GaP, GaAsP, InAs, InP, AlGaAs, or InAsP. Other dopants may also be included with these materials and combinations thereof, for example, transition metals such as Fe, Co, Te, Au, and the like. As used herein, transition metal groups of the periodic table, when referred to in isolation (i.e., without referring to the main group elements), are indicated with a "B." The transition metals elements include the Group IB elements (Cu, Ag, Au), the Group IIB elements

(Zn, Cd, Hg), the Group IIIB elements (Sc, Y, lanthanides, actinides), the Group IVB elements (Ti, Zr, Hf), the Group VB elements (V, Nb, Ta), the Group VIB elements (Cr, Mo, W), the Group VIIB elements (Mn, Tc, Re), and the Group VIIIB elements (Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt).

As used herein, a "semiconductor" is given its ordinary meaning in the art, i.e., an element having semiconductive or semi-metallic properties (i.e., between metallic and non-metallic properties). An example of a semiconductor is silicon. Other non-limiting examples include gallium, germanium, diamond (carbon), tin, selenium, tellurium, boron, or phosphorous.

In one set of embodiments, the invention includes a nanoscale wire (or other nanostructured material) that is a single crystal. As used herein, a "single crystal" item (e.g., a semiconductor) is an item that has covalent bonding, ionic bonding, or a combination thereof throughout the item. Such a single-crystal item may include defects in the crystal, but is to be distinguished from an item that includes one or more crystals, not ionically or covalently bonded, but merely in close proximity to one another. Techniques for producing such nanoscale wires are further discussed below.

The nanoscale wire may also have certain novel physical properties in some embodiments. The enhanced physical properties of the nanoscale wires of the invention may be due to the crystallinity of the nanowires (for example, a nanoscale wire having very few crystal domains, and in some cases, the nanoscale wire being a single crystal), quantum effects (e.g., due to the size of the nanoscale wire), or the like. For instance, in some cases, a nanoscale wire of the invention may have very low resistivities, for example, resistivities of less than about 100 microOhm cm ($\mu\Omega$ cm) and in some cases, less than about 80 microOhm cm, less than about 60 microOhm cm, less than about 40 microOhm cm, less than about 20 microOhm cm or less than about 10 microOhm cm. In another set of embodiments, the nanowire of the invention may be able to carry very high current densities without breakage or mechanical failure. For example, a nanowire of the invention may be able to carry current densities of at least about $10^7 A/cm^2$, and in some cases, greater than about $10^8 A/cm^2$, or greater than about $10^9 A/cm^2$ without breakage or mechanical failure.

In another set of embodiments, the nanoscopic wire (or other nanostructured material) comprising a metal-semiconductor compound may include additional materials, such as semiconductor materials, dopants, organic compounds, inorganic compounds,

etc. The following are non-limiting examples of materials that may be used as dopants within the nanoscopic wire. The dopant may be an elemental semiconductor, for example, silicon, germanium, tin, selenium, tellurium, boron, diamond, or phosphorous. The dopant may also be a solid solution of various elemental semiconductors. Examples include a mixture of boron and carbon, a mixture of boron and $P(BP_6)$, a mixture of boron and silicon, a mixture of silicon and carbon, a mixture of silicon and germanium, a mixture of silicon and tin, a mixture of germanium and tin, etc. In some embodiments, the dopant may include mixtures of Group IV elements, for example, a mixture of silicon and carbon, or a mixture of silicon and germanium. In other embodiments, the dopant may include mixtures of Group III and Group V elements, for example, BN, BP, BAs, AlN, AlP, AlAs, AlSb, GaN, GaP, GaAs, GaSb, InN, InP, InAs, or InSb. Mixtures of these combinations may also be used, for example, a mixture of BN/BP/BAs, or BN/AlP. In other embodiments, the dopants may include mixtures of Group III and Group V elements. For example, the mixtures may include AlGaN, GaPAs, InPAs, GaInN, AlGaInN, GaInAsP, or the like. In other embodiments, the dopants may also include mixtures of Group II and Group VI elements. For example, the dopant may include mixtures of ZnO, ZnS, ZnSe, ZnTe, CdS, CdSe, CdTe, HgS, HgSe, HgTe, BeS, BeSe, BeTe, MgS, MgSe, or the like. Alloys or mixtures of these dopants are also be possible, for example, ZnCd Se, or ZnSSe or the like. Additionally, mixtures of different groups of semiconductors may also be possible, for example, combinations of Group II-Group VI and Group III-Group V elements, such as $(GaAs)_x(ZnS)_{1-x}$. Other non-limiting examples of dopants may include mixtures of Group IV and Group VI elements, for example GeS, GeSe, GeTe, SnS, SnSe, SnTe, PbO, PbS, PbSe, PbTe, etc.. Other dopant mixtures may include mixtures of Group I elements and Group VII elements, such as CuF, CuCl, CuBr, CuI, AgF, AgCl, AgBr, AgI, or the like. Other dopant mixtures may include different mixtures of these elements, such as $BeSiN_2$, $CaCN_2$, $ZnGeP_2$, $CdSnAs_2$, $ZnSnSb_2$, $CuGeP_3$, $CuSi_2P_3$, Si_3N_4, Ge_3N_4, Al_2O_3, $(Al, Ga, In)_2(S, Se, Te)_3$, Al_2CO, $(Cu, Ag)(Al, Ga, In, Tl, Fe)(S, Se, Te)_2$ or the like.

As a particular non-limiting example, a p-type dopant may be selected from Group III, and an n-type dopant may be selected from Group V. For instance, a p-type dopant may include at least one of B, Al and In, and an n-type dopant may include at least one of P, As and Sb. For Group III-Group V mixtures, a p-type dopant may be selected from Group II, including one or more of Mg, Zn, Cd and Hg, or Group IV,

including one or more of C and Si. An n-type dopant may be selected from at least one of Si, Ge, Sn, S, Se and Te. It will be understood that the invention is not limited to these dopants, but may include other elements, alloys, or mixtures as well.

The nanoscale wire of the present invention may further include, in some cases, any organic or inorganic molecules. In some cases, the organic or inorganic molecules are polarizable and/or have multiple charge states. For example, the nanoscale wires may include gallium arsenide, gallium nitride, indium phosphide, germanium, or cadmium selenide.

In yet another set of embodiments, nanoscale wire (or other nanostructured material) may comprise two or more regions having different compositions. One or more of the regions may include a metal-semiconductor compound. Each region of the nanoscale wire may have any shape or dimension, and these can be the same or different between regions. For example, a region may have a smallest dimension of less than 1 micron, less than 100 nm, less than 10 nm, or less than 1 nm. In some cases, one or more regions may be a single monolayer of atoms (i.e., "delta-doping"). In certain cases, the region may be less than a single monolayer thick (for example, if some of the atoms within the monolayer are absent).

The two or more regions may be longitudinally arranged relative to each other, and/or radially arranged (e.g., as in a core/shell arrangement) within the nanoscale wire. As one example, the nanoscale wire may have multiple regions of semiconductor materials arranged longitudinally. In another example, a nanoscale wire may have two regions having different compositions arranged longitudinally, surrounded by a third region or several regions, each having a composition different from that of the other regions. As a specific example, the regions may be arranged in a layered structure within the nanoscale wire, and one or more of the regions may be delta-doped or at least partially delta-doped. As another example, the nanoscale wire may have a series of regions positioned both longitudinally and radially relative to each other. The arrangement can include a core that differs in composition along its length (changes in composition or concentration longitudinally), while the lateral (radial) dimensions of the core do, or do not, change over the portion of the length differing in composition. The shell portions can be adjacent each other (contacting each other, or defining a change in composition or concentration of a unitary shell structure longitudinally), or can be separated from each other by, for example, air, an insulator, a fluid, or an auxiliary, non-

nanoscale wire component. The shell portions can be positioned directly on the core, or can be separated from the core by one or more intermediate shells portions that can themselves be constant in composition longitudinally, or varying in composition longitudinally. That is, the invention allows the provision of any combination of a nanowire core and any number of radially-positioned shells (e.g., concentric shells), where the core and/or any shells can vary in composition and/or concentration longitudinally, any shell sections can be spaced from any other shell sections longitudinally, and different numbers of shells can be provided at different locations longitudinally along the structure.

As used herein, regions that differ in composition may comprise different materials or elements, and/or may comprise the same materials or elements, but at different ratios or concentrations. Each region may be of any size or shape within the nanoscale wire. Two regions positioned adjacent to each other define a junction therebetween. A junction within the nanoscale wire may be, for example, a p/n junction, a p/p junction, an n/n junction, a p/i junction (where i refers to an intrinsic semiconductor), an n/i junction, an i/i junction, or the like. The junction may also be a Schottky junction. The junction may also be a semiconductor/semiconductor junction, a semiconductor/metal junction, a semiconductor/insulator junction, a metal/metal junction, a metal/insulator junction, an insulator/insulator junction, or the like. The junction may also be a junction of two materials, a doped semiconductor to a doped or an undoped semiconductor, or a junction between regions having different dopant concentrations. The junction may also be a defected region to a perfect single crystal, an amorphous region to a crystal, a crystal to another crystal, an amorphous region to another amorphous region, a defected region to another defected region, an amorphous region to a defected region, or the like. More than two regions may be present within the nanoscale wire, and these regions may have unique compositions, or may comprise the same compositions. As one example, a wire may have a first region having a first composition, a second region having a second composition, and a third region having a third composition or the same composition as the first composition.

The regions of the nanoscale wire may be distinct from each other with minimal cross-contamination, or the composition of the nanoscale wire may vary gradually from one region to the next. In some embodiments, the junction between two differing regions (e.g., between different longitudinal regions between a core and shell, between

two different shells, etc.) may be "atomically-abrupt," where there is a sharp transition at the atomic scale between two adjacent regions that differ in composition. However, in other embodiments, the junction between two differing regions may be more gradual. For example, the "overlap region" between the adjacent regions may be a few nanometers wide, for example, less than about 500 nm, less than about 100 nm, less than about 50 nm, less than about 40 nm, less than about 20 nm, or less than about 10 nm. In certain instances, the overlap region between a first region having a composition and a second region having a composition different from the first region (i.e., different concentrations or different species) can be defined as the distance between where the composition of the overlap region ranges between about 10 vol% and about 90 vol% of the composition of the first region, with the remainder having a complementary amount of the composition of the second region. In certain embodiments of the invention, nanoscale wires having more than one junction between two regions having different compositions are also contemplated. For example, a nanoscale wire may have two, three, four, or more overlap regions. The number of periods and the repeat spacing may be constant or varied.

In some embodiments, a gradual change in composition between two adjacent regions may relieve strain and may enable defect-free junctions and superlattices. However, in other embodiments, atomically-abrupt interfaces may be desirable, for example, in certain photonic and electronic applications. The nature of the interface between the two adjacent regions may be controlled by any suitable method (as further described below), for example, by using different nanocluster catalysts or varying the growth temperature when reactants are switched during synthesis. Nanoscale wires having atomically-abrupt regions may be fabricated, for example, by reducing the diameter of the nanoscale wire by reducing the size of the starting nanocluster, or by controlling exposure of the growing wire to dopant gases, for example, by selectively purging or evacuating the region surrounding the wire between different gas exposures or reaction conditions.

If the nanoscale wire includes one or more shells, the shells can be of the same or different composition relative to each other, and any of the shells can be of the same composition of a segment of the core, or of a different composition, or can contain the same or different concentration of a dopant as is provided in a section of the core. The shells may be grown using any suitable growth technique, for example, including the

techniques described herein, such as CVD or LCG. The shells and/or cores of the nanoscale wires may be etched using any suitable technique, including the techniques described herein. As one example, in a nanoscale wire having a shell and a core region different from the shell region, after being assembled on a substrate, the shell may be selectively etched off from the nanoscale wire or chemically reacted on the nanoscale wire.

In another aspect, the present invention contemplates a wide variety of devices. Such devices may include electrical devices, optical devices, optronic devices, spintronic devices, mechanical devices or any combination thereof, for example, optoelectronic devices or electromechanical devices. Functional devices assembled from the nanoscale wires (or other nanostructured materials) described herein may be used to produce various computer or device architectures. For example, certain nanoscale wires described herein, such as those including one or more metal-semiconductor compounds, may be assembled into nanoscale versions of conventional semiconductor devices, such as diodes, light emitting diodes (LEDs), inverters, sensors, bipolar transistors, etc. These devices may include single, free-standing nanoscale wires, crossed nanoscale wires, or combinations of single nanoscale wires combined with other components. Nanoscale wires having different dopants, doping levels, or combinations of dopants may also be used in certain cases to produce these devices. The nanoscale wires, in particular cases, may also have multiple regions, each of which may have different compositions, as previously described. In some embodiments, a further step may include the fabrication of these structures within the nanoscale wires themselves, wherein a single nanoscale wire is able to operate as a functional devices. In other embodiments, a nanoscale wire may also be used as an interconnect between two devices, or between a device and an external circuit or system.

The present invention, in one set of embodiments, includes the ability to fabricate essentially any electronic device from adjacent n-type and p-type semiconducting components. This includes any device that one of ordinary skill in the art would desirably make using n-type and p-type semiconductors in combination. Examples of such devices include, but are not limited to, field effect transistors (FETs), bipolar junction transistors (BJTs), tunnel diodes, modulation doped superlattices, complementary inverters, light emitting devices, light sensing devices, biological system imagers, biological and chemical detectors or sensors, thermal or temperature detectors,

Josephine junctions, nanoscale light sources, photodetectors such as polarization-sensitive photodetectors, gates, inverters, AND, NAND, NOT, OR, XOR, and NOR gates, latches, flip-flops, registers, switches, clock circuitry, static or dynamic memory devices and arrays, state machines, gate arrays, and any other dynamic or sequential logic or other digital devices including programmable circuits. Also included are analog devices and circuitry, including but not limited to, amplifiers, switches and other analog circuitry using active transistor devices, as well as mixed signal devices and signal processing circuitry. Also included are p/n junction devices with low turn-on voltages, p/n junction devices with high turn-on voltages, and computational devices such as a half-adder. Furthermore, junctions having large dielectric contrasts between two regions may be used to produce 1D waveguides with built-in photonic band gaps, or cavities for nanoscale wire lasers. In some embodiments, the nanoscale wires of the present invention may be manufactured during the device fabrication process. In certain cases, nanoscale wires of the present inventions may first be synthesized, then assembled in a device.

In one embodiment, the invention includes a nanoscale inverter. In some cases, the inverter may be constructed using adjacent regions having different compositions, for example, a p-type and an n-type semiconductor region. For example, in one embodiment, the invention provides a lightly-doped complementary inverters (complementary metal oxide semiconductors) arranged by contact of an n-type semiconductor region with a p-type semiconductor region. The invention also provides lightly-doped complementary inverters (complementary metal oxide semiconductors) arranged by contact of an n-type semiconductor with a p-type semiconductor, for example, by arrangement of crossed n-type and p-type semiconducting nanoscale wires, or by the arrangement of two adjacent regions.

The invention includes a nanoscale diode according to another embodiment. In some cases, the invention provides a diode constructed using adjacent regions having different compositions, for example, a p-type and an n-type semiconductor region, for example, Zener diodes, tunnel diodes, light-emitting diodes, and the like. For example, the diode may be a tunnel diodes heavily-doped with semiconducting components. A tunnel diode may be arranged similarly or exactly the same as a complementary inverter, with the semiconductors being heavily doped rather than lightly doped.

In yet another embodiment, the invention comprises a nanoscale transistor, such as a field effect transistor ("FET") or a bipolar junction transistor ("BJT"). The transistor may have a smallest width of less than 500 nm, less than 100 nm, or any other width as described herein. In one set of embodiments, the transistor may be constructed using adjacent regions having different compositions. As an example, a p-type and an n-type semiconductor region may be contemplated, for example, arranged longitudinally within a single wire, arranged radially within the wire, between adjacent crossed wires, and the like, as well as combinations of these. In some embodiments, the transistor may comprise a doped semiconductor, such as a p-type or n-type semiconductor, as is known by those of ordinary skill in the art in transistor fabrication. The present invention, in some cases, also contemplates controlled doping of nanoscale wires such that a fabrication process can involve fabricating functional FETs according to a technique in which much greater than one in fifty devices is functional. For example, the technique can involve preparing a doped nanoscale wire and fabricating an FET therefrom.

A FET comprising a nanoscale wire may serve as a conducting channel in some cases, and an elongated material having a smallest width of less than 500 nm (e.g., a nanoscale wire) serving as the gate electrode. For such a FET, the widths of the nanoscale wire and the elongated material may define a width of the FET. The field effect transistor may also, in some instances, comprise a doped or intrinsic semiconductor having at least one portion having a smallest width of less then 500 nanometers, and a gate electrode comprising an elongated material having at least one portion having a smallest width of less then 500 nanometers. Furthermore, in some cases, the nanoscale wire may comprise a semiconductor, and/or have a core/shell arrangement, and such a shell may function as a gate dielectric for the FET. In certain instances, the two regions may be longitudinally positioned. In certain cases, the intersection of a nanoscale wire and an elongated material may define a length of the FET. The transistor may also be a coaxially-gated transistor in some cases. In some cases, the FETs are readily integratable into devices, and the assembly of such FETs may be shrunk in a straightforward manner into nanometers scale. Such a "bottom-up" approach may scale down to sizes far beyond what is predicted for traditional "top-down" techniques typically used in the semiconductor industry today. Further, such bottom-up assembly may prove to be cheaper than the traditional top-down approach.

In another set of embodiments, various electronic devices incorporating the nanoscale wires of the invention may be controlled, for example, using any input signal, such as an electrical, optical or a magnetic signal. The control may involve switching between two or more discrete states, or may involve continuous control of nanoscale wire current, i. e., analog control. In addition to electrical signals, optical signals and magnetic signals, the devices may also be controlled in certain embodiments in response to biological and chemical species, for example, DNA, protein, metal ions, peptides, etc. Any species that is charged or has a dipole moment may be detected in some cases. In other embodiments, the device may be switchable in response to mechanical stimuli, for example, mechanical stretching, vibration and bending. In yet other embodiments, the device may be switchable in response to an external physical stimulus such as temperature, pressure, or fluid movement, for example, the movement of an environmental gas or liquid.

In yet another set of embodiments, devices including nanoscale wires having more than one region able to produce or emit light are contemplated. For example, a nanoscale wire having multiple p-type and n-type regions which may be produced, where each p/n junction is able to emit light. The nanoscale wire may have two, three, four, five, or more p/n junctions. The number of periods and the repeat spacing between each p/n junction may be constant or varied during growth. Thus, for example, nanoscale wires having multiple light-emitting and non-light-emitting regions may be used as "nano-bar codes," where different sequences, patterns, and/or frequencies of light-emitting and non-light-emitting regions may be used to uniquely "tag" or label an article that the nanoscale wire is used in. Varying the composition of each p/n junction (for example, by using different dopants) may alter the frequency of the emitted light; thus, additional information can be encoded through variations in the color of the emitting region using multi-component superlattices in certain instances.

In still another set of embodiments, a device including nanoscale wire may be used as a photodetector. In some cases, the responsivity of the nanophotodetector may be greater than about 1000 A/W, greater than about 3000 A/W, still greater than about 5000 A/W, or greater than about 10000 A/W. In certain embodiments, the response time of the semiconductor photodetector may be less than 1 ps, less than about 100 fs, less than about 10 fs, or still less than about 1 fs, due to the small capacitances of the nanoscale wires, which may be less than about 100 aF or about 10 aF in some cases.

Electrically erasable and re-writable memory structures and devices with reversible states and good retention time may be constructed using the nanoscale wires of the invention, according to another set of embodiments. When the surfaces of these devices are appropriately modified with either molecules or nanocrystals, reversible memory switching behavior may be observed when electrical pulses of opposite polarity is applied. Specifically, subjection to positive or negative voltage pulses in either gate or bias voltages may cause the devices to make fully reversible transition between low-resistance and high resistance states. In some cases, the transition between states is performed directly, through the flow of electrons through the device or component. In other cases, the transition between states is accomplished inductively, through the use of field effects, electron tunneling, or the like.

In some cases, nanoscale memory switching device may be assembled from one or more nanoscale wires described herein. The memory switching device may have multiple states, non-volatile reversible states, or a large on/off ratio in some instances. The nanoscale memory switching devices may be highly parallel and scalable with simple chemical assembly process, and can be useful in construction of a chemically assemble computer in some embodiments.

The memory switching device, in one embodiment, is a three terminal devices based on individual nanoscale wires using the gate pulse to induce the switching between two states, such as between high- and low-resistance states. In another embodiment, the memory switching device is a two terminal devices based on individual nanoscale wires using the bias pulse to induce the switching between high- and low-resistance states. In yet another embodiment, the memory switching device is based on the junction between two regions having different compositions, for example, in a core/shell arrangement, in an arrangement where the two regions are longitudinally positioned relative to each other, in arrangements having crossed nanoscale wire p-n junctions, etc. A bias pulse or a gate pulse may be used to induce switching between high- and low resistance states, for example, by supplying a charge or a current through the nanoscale wire or a region thereof, such as through a core region. In still another embodiment, the memory switching device may have three, four, six, eight, or other multiple states or configurations.

In some cases, memory systems using the nanoscale wires of the invention may take the form of novel structures such as two-dimensional parallel, crossing, or three-

dimensional stacked memory arrays to achieve ultra-high density data storage, and non-volatile state switches for computer systems fabricated by chemical assembly. Thus, it is possible to achieve an active element two-dimensional density of at least 10^{11} memory elements/cm^2, preferably at least about 10^{12} memory elements/cm^2. For example, using nanoscale wires of 10 micron length, with a memory element every 20 nm along each nanoscale wire, an array can be formed with 500 parallel wires in each direction, each wire containing 500 crossbar array junctions (memory elements). For instance, 250,000 memory elements may be formed in such an array. Three-dimensional arrays can be created as well, in some instances. For example, where a 1 micron spacing is created between two-dimensional array planes, the invention provides a three-dimensional array density of at least about 10^{14} memory elements/cm^3, and in some cases, at least about 10^{15} memory elements/cm^3 or more.

The invention, in yet another set of embodiments, provides a sensing element. The sensing element may be an electronic sensing element, and the sensing element may include a nanoscale wire able to detect the presence, absence, and/or amount (concentration), of a species such as an analyte in a sample (e.g. a fluid sample) containing, or suspected of containing, the species. Nanoscale sensors of the invention may be used, for example, in chemical applications to detect pH or the presence of metal ions; in biological applications to detect a protein, nucleic acid (e.g. DNA, RNA, etc.), a sugar or carbohydrate, and/or metal ions; and in environmental applications to detect pH, metal ions, or other analytes of interest. Also provided, according to another embodiment, is an article comprising a nanoscale wire and a detector constructed and arranged to determine a change in an electrical property of the nanoscale wire. At least a portion of the nanoscale wire is addressable by a sample containing, or suspected of containing, an analyte. The phrase "addressable by a fluid" is defined as the ability of the fluid to be positioned relative to the nanoscale wire so that an analyte suspected of being in the fluid is able to interact with the nanoscale wire. The fluid may be proximate to or in contact with the nanoscale wire.

The nanoscale wire, in certain cases, may be chosen on the basis of its ability to interact with an analyte, i.e., whether the appropriate reaction entity, e.g. a binding partner, can be easily attached to the surface of the nanoscale wire, and/or whether the appropriate reaction entity, e.g. a binding partner, can be positioned near the surface of the nanoscale wire. The selection of suitable nanostructures, e.g., conductors or

semiconductors, nanotubes or nanoscale wires, will be apparent and readily reproducible by those of ordinary skill in the art with the benefit of the present disclosure. The term "binding partner," as used herein, refers to a molecule that can undergo binding with a particular molecule. Biological binding partners are examples. Non-limiting examples include nucleic acid-nucleic acid binding, nucleic acid-protein binding, protein-protein binding, enzyme-substrate binding, receptor-ligand binding, receptor-hormone binding, antibody-antigen binding, etc.

In some cases, chemical changes associated with a nanoscale wires can be used to modulate the properties of the nanoscale wires to create electronic devices of a variety of types. The presence of an analyte can change the electrical properties of the nanoscale wires, e.g., through electrocoupling with a binding agent of the nanoscale wire. If desired, the nanoscale wires may be coated with a specific reaction entity, binding partner or specific binding partner, chosen for its chemical or biological specificity to a particular analyte.

The reaction entity may be positioned relative to the nanoscale wire to cause a detectable change in the nanoscale wire. In some cases, the reaction entity may be positioned within 100 nm of the nanoscale wire, within 50 nm of the nanoscale wire, or within 10 nm of the nanoscale wire. The actual proximity can be determined by those of ordinary skill in the art. In one embodiment, the reaction entity is positioned less than 5 nm from the nanoscopic wire. In other embodiments, the reaction entity is positioned with 4 nm, 3 nm, 2 nm, and 1 nm of the nanoscopic wire. In one embodiment, the reaction entity is attached to the nanoscopic wire through a linker.

The invention, in another embodiment, provides an article comprising a sample exposure region and a nanoscale wire able to detect the presence or absence of an analyte, and/or the concentration of the analyte. The sample exposure region may be any region in close proximity to the nanoscale wire wherein a sample in the sample exposure region addresses at least a portion of the nanoscale wire. Examples of sample exposure regions include, but are not limited to, a well, a channel, a microchannel, and a gel. In certain embodiments, the sample exposure region is able to hold a sample proximate the nanoscale wire, and/or may direct a sample toward the nanoscale wire for determination of an analyte in the sample. The nanoscale wire may be positioned adjacent to or within the sample exposure region. Alternatively, the nanoscale wire may be a probe that is inserted into a fluid or fluid flow path. The nanoscale wire probe may also comprise a

microneedle and the sample exposure region may be addressable by a biological sample. In this arrangement, a device that is constructed and arranged for insertion of a microneedle probe into a biological sample will include a region surrounding the microneedle that defines the sample exposure region, and a sample in the sample exposure region is addressable by the nanoscale wire, and vice versa. Fluid flow channels can be created at a size and scale advantageous for use in the invention (microchannels) using a variety of techniques such as those described in International Patent Publication No. WO 97/33737, published September 18, 1997, and incorporated herein by reference.

In yet another aspect, the present invention provides a method of preparing a nanostructure. In one set of embodiments, the method involves allowing a first material to diffuse into at least part of a second material, optionally creating a new compound. In some cases, diffusion may proceed until at least part of the first material reaches a center portion of the first material, or until the first material has been incorporated substantially throughout the second material (e.g., the second material has been "bulk-doped" with the first material). The first and second materials may each be metals or semiconductors, one material may be a metal and the other material may be a semiconductor, etc. Diffusion of the first material in the second material may occur, in one set of embodiments, passively or spontaneously, i.e., no external conditions may be necessary to cause the first material to diffuse into the second material. In another set of embodiments, diffusion of the first material into the second material may occur under external conditions related to those involved in the formation and/or positioning of the first and/or second materials. In yet another set of embodiments, the first material may be unable to diffuse into the second material under normal or ambient conditions (for example, under room temperature and/or pressure), or under conditions involved in the formation and/or positioning of the first and/or second materials, but diffusion of the first material into the second material may be initiated and/or facilitated by the application of suitable external conditions able to promote diffusion, for example, increases in temperature and/or pressure. In still another set of embodiments, diffusion of the first material into the second material may be initiated by applying an external stimulus, for example, by altering the temperature and/or pressure, by removing an intervening layer positioned between the first material and the second material, or the like. It should be understood that "diffuse," as used herein, refers to diffusion processes

that occurs on detectable time scales of interest, e.g., the migration of the atoms of a first material into a second material on the nanoscale may be detectable within about an hour, using techniques known to those of ordinary skill in the art (for example, electron or optical microscopy, measurements of resistivity or conductivity, etc.). In many cases, the migration of the atoms of the first material into the second material may be detected within about 30 minutes, within about 15 minutes, within about 10 minutes, or within about 5 minutes. Thus, as an example, diffusion may be allowed to proceed until the conductivity of the second material has been substantially altered, for instance, such that the conductivity of the second material has been altered from that of a semiconductor to that of a conductor (or vice versa), etc.

The nanostructure, after the first material has diffused into at least part of the second material, may have any of the structures described herein, for example, a single crystal wire, a wire comprising a core/shell heterojunction, a wire comprising a longitudinal heterojunction, a device comprising a wire, or the like. The materials for the nanostructure may be chosen such that the diffusing material is able to diffuse into at least an interior portion of the receiving material, i.e., internally of the surface of the receiving material. The method, in some cases, may be used to prepare a nanostructure comprising a metal-semiconductor compound such as a metal silicide. One or more of any of the following-described methods may also be used in the preparation of a nanostructure comprising a metal-semiconductor compound.

In one embodiment, a first material is positioned adjacent or proximate to a second material (by known forms of deposition, for example), and the atoms of the first material are allowed to diffuse into at least a portion of the second material. At least one of the first and second materials may be a nanoscale material. Thus, as an example, in Fig. 5A, a first material 51 is positioned next to a second material 52. The first material may be positioned such that it contacts the second material, and/or such that atoms from the first material are able to diffuse into the second material (for example, an intervening material or space may be present between the first material and the second material). Diffusion of the first material into at least a portion of the second material is then allowed to occur, as shown in Fig. 5B. When sufficient diffusion has occurred (i.e., when a desired amount of the first material has diffused into the second material), the first material (or at least a portion thereof) may optionally be removed, as is shown in Fig. 5C.

For example, to create a nanoscale wire comprising a metal-semiconductor compound, a metal may be positioned adjacent or proximate to a semiconductor (by known forms of deposition, for example), and the metal atoms allowed to diffuse into at least a portion of the semiconductor material, for example, to create one or more heterojunctions within the nanoscale wire. The metal may be a bulk metal in some cases, i.e., a metal having a volume of at least nanoscopic dimensions (e.g., having a smallest dimension of at least about 1 nm).

In some cases, diffusion of the metal atoms into the semiconductor may be initiated and/or facilitated, for example, by the application of high pressures and/or high temperatures, for example, temperatures of at least about 500°C, at least about 550°C, at least about 600°C, at least about 700°C, or more in some cases. In certain instances, substantial diffusion of metal atoms into the semiconductor may not substantially occur absent an increase or an alteration in the temperature and/or pressure. In some cases, diffusion of the metal atoms into the semiconductor (or at least a portion thereof) may proceed until a metal-semiconductor compound forms (e.g., through a chemical reaction), and/or when a stoichiometric ratio of metal atoms to semiconductor atoms has been established. As a particular example, if the metal is a transition metal such as nickel, and the semiconductor material is silicon nanoscale wire, diffusion of nickel into the silicon nanoscale wire may proceed until the silicon nanoscale wire (or at least that portion of the nanoscale wire exposed to nickel) has been converted into a nickel silicide nanoscale wire. In other cases, however, the metal atoms and the semiconductor atoms may not be in a stoichiometric ratio. In certain instance, diffusion of the metal into the semiconductor may be stopped before metal-semiconductor compound formation or stoichiometric equilibrium has been established, thus, in one embodiment, the nanoscale wire may include a non-stoichiometric ratio of metal atoms to semiconductor atoms.

After the metal atoms have been allowed to diffuse into the semiconductor, in some cases, excess metal may be removed from the semiconductor, for example, by the application of certain species such as metal etchants. For example, if the metal diffused into the semiconductor is nickel, a suitable metal etchant may include acids such as nitric acid, sulfuric acid, hydrochloric acid, and/or nickel etchants such as TFB or TFG (available from Transene, Danvers, MA). In some cases, the removal of the excess metal from the semiconductor may be facilitated by elevated temperatures and/or pressures.

In another set of embodiments, a nanostructure can be prepared by exposing a portion of the second material to the first material. The first material can diffuse into regions of the second material that are adjacent or proximate the first material, while regions of the second material not adjacent or proximate the first material will remain substantially free of the first material. As one example, as shown in Fig. 3A, a mask 38 may be patterned on a nanostructure 37 (or other nanostructure) to define one or more regions where the nanostructure is covered by the mask 60 and one or more regions where the nanostructure is free of the mask 65. The mask may have any pattern defined therein, and can define 2- or 3-dimensional patterns on the nanostructure, depending on the specific application. Any suitable material may be used to form the mask, for instance, a photoresist may be formed on the nanostructure to define a mask, e.g., through photolithographic techniques known to those of ordinary skill in the art. As a non-limiting example, a mask with a series of openings may be formed on a nanowire to create a series of heterojunctions along the nanowire, or if not formed on the nanowire (or other nanostructure), positioned in proximity relative to the nanowire so as to be able to mask application of material on the nanowire. As another example, a mask may be formed from a nanoscale wire, for example, a nanoscale wire, a nanotube, a core/shell nanoscale wire, etc. For instance, the nanoscale wire used as a mask may be placed on or positioned in proximity to the nanowire (or other nanostructure); the nanoscale wire used as a mask may thus mask application of material on the nanowire.

After positioning of the mask on the second material of the nanostructure, or between the nanostructure and the source of material to be deposited thereto, the first material may be deposited on the mask. Regions of the nanostructure that are free of the mask 65 will have the first material deposited thereon, while regions of the nanostructure covered by the mask 60 will not be exposed to the first material. The first material can then diffuse into the portions second material adjacent or proximate the first material. The mask may be removed before or after diffusion of the first material into portions of the second material. After diffusion, a nanostructure having one or more heterojunctions 67, defined by the mask, can be created.

In yet another set of embodiments, the present invention involves controlling and altering the doping of semiconductors in a nanoscale wire. In some cases, the nanoscale wires (or other nanostructure) may be produced using techniques that allow for direct and controlled growth of the nanoscale wires. For instance, the direct growth of doped

nanoscale wires may eliminate the need to use lithographic steps during production of the nanoscale wire, thus facilitating the "bottom-up" assembly of complex functional structures. Fabrication paradigms for single nanoscale wire devices that are contemplated in the present invention include, but are not limited to, direct fabrication of nanoscale wire junctions during synthesis, or doping of nanoscale wires via post-synthesis techniques (e. g., annealing of dopants from contacts or solution-processing techniques). The dopants may be changed at any point during the growth of the nanoscale wire.

In some cases, the nanoscale wire may be doped during growth of the nanoscale wire. Doping the nanoscale wire during growth may result in the property that the doped nanoscale wire is bulk-doped. Furthermore, such doped nanoscale wires may be controllably doped, such that a concentration of a dopant within the doped nanoscale wire can be controlled and therefore reproduced consistently, making possible the commercial production of such nanoscale wires. Additionally, the dopant may be systematically altered during the growth of the nanoscale wire, for example, so that the final nanoscale wire has a first doped region comprising a first dopant and a second doped region differing in composition from the first region, for example, by comprising a second dopant, comprising the first dopant at a different concentration, or omitting the first dopant.

Certain embodiments of the invention may utilize metal-catalyzed CVD techniques ("chemical vapor deposition") to synthesize individual nanoscale wires. CVD synthetic procedures useful for preparing individual wires directly on surfaces and in bulk form are generally known, and can readily be carried out by those of ordinary skill in the art. See, for example, Kong, *et al.*, "Synthesis of Individual Single-Walled Carbon Nanotubes on Patterned Silicon Wafers," *Nature*, 395:878-881 (1998); or Kong, *et al.*, "Chemical Vapor Deposition of Methane for Single-Walled Carbon Nanotubes," *Chem. Phys. Lett.*, 292:567-574 (1998). Nanoscopic wires may also be grown through laser catalytic growth. See, for example, Morales, *et al.*, "A Laser Ablation Method for the Synthesis of Crystalline Semiconductor Nanowires," *Science*, 279:208-211 (1998). With the same basic principles as LCG, if uniform diameter nanoclusters (less than 10-20% variation depending on how uniform the nanoclusters are) are used as the catalytic cluster, nanoscale wires with uniform size (diameter) distribution can be produced, where the diameter of the nanoscale wires is determined by the size of the catalytic

clusters. By controlling the growth time, nanoscale wires with different lengths can be grown.

One technique that may be used to grow nanoscale wires is catalytic chemical vapor deposition ("C-CVD"). In the C-CVD method, the reactant molecules are formed from the vapor phase, as opposed to from laser vaporization. In C-CVD, nanoscale wires may be doped by introducing the doping element into the vapor phase reactant (e. g. diborane and phosphane for p-type and n-type doped regions). The doping concentration may be controlled by controlling the relative amount of the doping compound introduced in the composite target. The final doping concentration or ratios are not necessarily the same as the vapor-phase concentration or ratios. By controlling growth conditions, such as temperature, pressure or the like, nanoscale wires having the same doping concentration may be produced. To produce a nanoscale wire having adjacent regions having different compositions within a nanoscale wire, the doping concentration may be varied by simply varying the ratio of gas reactant (e. g. from about 1 ppm to about 10%, from about 10 ppm to about 20%, from about 100 ppm to about 50%, or the like), or the types of gas reactants used may be altered during growth of the nanoscale wire. The gas reactant ratio or the type of gas reactants used may be altered several times during growth of the nanoscale wire, which may produce nanoscale wires comprising regions having multiple compositions, all of which may or may not be unique.

Another technique for direct fabrication of nanoscale wire junctions during synthesis is generally referred to as laser catalytic growth ("LCG"). In laser catalytic growth, dopants are controllably introduced during vapor phase growth of nanoscale wires. Laser vaporization of a composite target composed of a desired material (e. g. silicon or indium phosphide) and a catalytic material (e. g. a nanoparticle catalyst) may create a hot, dense vapor. The vapor may condenses into liquid nanoclusters through collision with a buffer gas. Growth may begin when the liquid nanoclusters become supersaturated with the desired phase and can continue as long as reactant is available. Growth may terminate when the nanoscale wire passes out of the hot reaction zone or when the temperature is decreased. The nanoscale wire may be further subjected to different semiconductor reagents during growth.

The catalytic materials and/or the vapor phase reactants may be produced by any suitable technique. For example, laser ablation techniques may be used to generate catalytic clusters or vapor phase reactant that may be used during LCG. Other

techniques are also contemplated, such as thermal evaporation techniques. The laser ablation technique may generate liquid nanoclusters that may subsequently define the size and direct the growth direction of the nanoscopic wires. The diameters of the resulting nanoscale wires may be determined by the size of the catalyst cluster, which in turn may be determined using routine experiments that vary the growth conditions, such as background pressure, temperature, flow rate of reactants, and the like. For example, lower pressure generally produces nanoscale wires with smaller diameters. Further diameter control may be achieved by using uniform diameter catalytic clusters.

As an example, vapor phase semiconductor reactants required for nanoscale wire growth may be produced by laser ablation of solid targets, vapor-phase molecular species, or the like. Any catalyst able to catalyze the production of nanoscale wires may be used. Gold may be preferred in certain embodiments. A wide range of other materials may also be contemplated, for example, a transition metal such as silver, copper, zinc, cadmium, iron, nickel, cobalt, and the like. Generally, any metal able to form an alloy with the desired semiconductor material, but does not form a more stable compound than with the elements of the desired semiconductor material may be used as the catalyst. The buffer gas may be any inert gas, for example, N_2 or a noble gas such as argon. In some embodiments, a mixture of H_2 and a buffer gas may be used to reduce undesired oxidation by residual oxygen gas.

A reactive gas used during the synthesis of the nanoscale wire may also be introduced when desired, for example, ammonia for semiconductors containing nitrogen. Nanoscale wires may also be flexibly doped by introducing one or more dopants into the composite target, for example, a germanium alloy during n-type doping of InP. The doping concentration may be controlled by controlling the relative amount of doping element, for example, between 0 and about 10% or about 20%, introduced in the composite target.

Laser ablation may generate liquid nanoclusters that subsequently define the size and direct the growth direction of the nanoscale wires. The diameters of the resulting nanoscale wires are determined by the size of the catalyst cluster, which may be varied by controlling the growth conditions, such as the pressure, the temperature, the flow rate and the like. For example, lower pressure may produce nanoscale wires with smaller diameters in certain cases. Further diameter control may be performed by using uniform diameter catalytic clusters.

If substantially uniform diameter nanoclusters (less than 10% to 20% variation depending on how uniform the nanoclusters are) are used as the catalytic material, nanoscale wires with substantially uniform size (diameter) distribution can be produced, where the diameter of the nanoscale wires generally is determined by the size of the catalytic material. By controlling the growth time or the position of the sample within the reactor, nanoscale wires with different lengths or different shell thicknesses may be grown.

To create a single junction within a nanoscale wire, in one set of the embodiments, the addition of the first reactant may be stopped during growth, and then a second reactant may be introduced for the remainder of the synthesis. This can be done abruptly, or a gradual change between reactants can be made, to result in an abrupt or gradual junction. Repeated modulation of the reactants, optionally with different reactants, during growth is also contemplated, which may produce nanoscale wire superlattices. LCG also may require a nanocluster catalyst suitable for growth of the different super lattice components, for example, a gold nanocluster catalyst can be used in a wide range of metal-semiconductor nanoscale wires, as well as Group III-V and Group IV materials. Substantially monodisperse metal nanoclusters may be used to control the diameter, and, through growth time, the length various semiconductor nanoscale wires.

As another example, LCG methods may be used to create nanoscale wires having a multishell configuration. For example, by altering the synthetic conditions during laser catalytic growth, homogeneous reactant decomposition may occur on the surface of the nanoscale wire. Control of the synthetic conditions may lead to a shell forming on the surface of the nanoscale wire, and in some embodiments, the synthetic reaction conditions may be controlled to cause the formation of a thin, uniform shell, a shell having a thickness of one atomic layer, or less in some cases. In other embodiments, by modulating or altering the reactants within the laser catalytic growth system, more than one shell may be built up on the outer surface of the nanoscale wire. As one none limiting example, a nickel silicide nanoscale wire core may be grown, and additional semiconductor materials may be deposited onto the surface, for example, a germanium shell, or a silicon shell doped with a dopant such as boron, or other dopants as described elsewhere in this application. The boundaries between the shells may be atomically abrupt, or may be graduated in some fashion, depending on how reactants such as, for

example, silane, germane, or diborane are introduced into the laser catalytic growth system. Arbitrary sequences of Si, Ge, NiSi, and alloy overlayers on both Si and Ge nanowire cores may also be prepared. Thus, a nanoscale wire having a core/shell arrangement may comprise a metal-semiconductor compound such as a metal silicide in the core and/or in at least one shell, or both in some cases. Other factors may contribute to the growing nanoscale wire, such as, for example, the reaction temperature, or the sample position within the furnace. By varying these parameters, the ratio of axial growth to radio growth may be controlled as desired.

In some cases, this methodology allows the direct formation of adjacent regions having different compositions within a nanoscale wire, such as a p/n junction, and/or adjacent regions differing in concentration of a particular element or composition. LCG also allows the creation of semiconductor superlattices, in which multiple layers of different composition are grown, which may give rise to a one-dimensional analog of multiple quantum states that are well known from thin-film studies. Alteration of the semiconductor reagents may allow for the formation of abrupt or gradual changes in the composition of the growing semiconductor material, allowing heterostructured materials to be synthesized. One non-limiting example of an LCG-grown semiconductor is a NiSi/GaAs heterojunction, which includes an initial growth of NiSi, followed by subsequent GaAs growth, giving an abrupt junction within a single nanoscale wire.

Other techniques to produce nanoscale semiconductors such as nanoscale wires are also within the scope of the present invention. For example, nanoscale wires of any of a variety of materials may be grown directly from vapor phase through a vapor-solid process. Also, nanoscale wires may also be produced by deposition on the edge of surface steps, or other types of patterned surfaces. Further, nanoscale wires may be grown by vapor deposition in or on any generally elongated template. The porous membrane may be porous silicon, anodic alumina, a diblock copolymer, or any other similar structure. The natural fiber may be DNA molecules, protein molecules carbon nanotubes, any other elongated structures. For all the above described techniques, the source materials may be a solution or a vapor. In some embodiments, while in solution phase, the template may also include be column micelles formed by surfactant molecules in addition to the templates described above.

In some cases, the nanoscale wire may be doped after formation. In one technique of post-synthetic doping of nanoscale wires, a nanoscale wire having a

substantially homogeneous composition is first synthesized, then is doped post-synthetically with various dopants. Such doping may occur throughout the entire nanoscale wire, or in one or more portions of the nanoscale wire, for example, in a wire having multiple regions differing in composition. Thus, as a specific non-limiting example, a semiconductor nanoscale wire may be prepared, then one or more regions of the nanoscale wire may be exposed to a dopant, thus resulting in a semiconductor nanoscale wire having a series of undoped semiconductor regions and doped semiconductor regions. As another example, a p/n junction can be created by introducing p-type and an n-type dopants down onto a single nanoscale wire. The p/n junction can then be further annealed in some cases to allow the dopants to migrate further into the nanoscale wire to form a bulk-doped nanoscale wire.

The following U.S. provisional and utility patent applications are incorporated herein by reference in their entirety for all purposes: Serial No. 60/524,301, entitled, "Nanoscale Arrays and Related Devices," filed November 20, 2003; Serial No. 10/196,337, entitled, "Nanoscale Wires and Related Devices," filed July 16, 2002, published as Publication No. 2003/0089899 on May 15, 2003; Serial No. 10/152,490, entitled, "Nanoscale Wires and Related Devices," filed May 20, 2002; Serial No. 60/226,835, entitled, "Semiconductor Nanowires," filed August 22, 2000; Serial No. 60/254,745, entitled, "Nanowire and Nanotube Nanosensors," filed December 11, 2000; Serial No. 60/292,035, entitled "Nanowire and Nanotube Nanosensors," filed May 18, 2001; Serial No. 60/292,121, entitled, "Semiconductor Nanowires," filed May 18, 2001; Serial No. 60/292,045, entitled "Nanowire Electronic Devices Including Memory and Switching Devices," filed May 18, 2001; Serial No. 60/291,896, entitled "Nanowire Devices Including Emissive Elements and Sensors," filed May 18, 2001; Serial No. 09/935,776, entitled "Doped Elongated Semiconductors, Growing Such Semiconductors, Devices Including Such Semiconductors, and Fabricating Such Devices," filed August 22, 2001, published as Publication No. 20020130311 on September 19, 2002; Serial No. 10/020,004, entitled "Nanosensors," filed December 11, 2001, published as Publication No. 20020117659 on August 29, 2002; Serial No. 60/348,313, entitled "Transistors, Diodes, Logic Gates and Other Devices Assembled from Nanowire Building Blocks," filed November 9, 2001; Serial No. 60/354,642, entitled "Nanowire Devices Including Emissive Elements and Sensors," filed February 6, 2002; and Serial No. 60/544,800, entitled "Nanostructures Containing Metal-Semiconductor Compounds," filed February

13, 2004. The following International Patent Publications are incorporated herein by reference in their entirety for all purposes: Application Serial No. PCT/US01/26298, entitled "Doped Elongated Semiconductors, Growing Such Semiconductors, Devices Including Such Semiconductors, and Fabricating Such Devices," filed August 22, 2001, published as Publication No. WO 02/17362 on February 28, 2002; Application Serial No. PCT/US01/48230, entitled "Nanosensors," filed December 11, 2001, published as Publication No. WO 02/48701 on June 20, 2002; Application Serial No. PCT/US02/16133, entitled "Nanoscale Wires and Related Devices." filed May 20, 2002, published as Publication No. WO 03/005450 on January 16, 2003.

The following examples are intended to illustrate certain aspects of certain embodiments of the present invention, but do not exemplify the full scope of the invention.

EXAMPLE 1

This example illustrates the preparation of single-crystal NiSi nanowires, according to one embodiment of the invention. With reference to Fig. 1A, silicon nanowires were synthesized via chemical vapor deposition using monodisperse gold nanocluster catalysts (Ted Pella) as catalysts and silane (SiH_4) as vapor-phase reactant, using previously reported techniques (nanowire 11 in Fig. 1A). The nanowire was determined to have a substantially uniform diameter. Next, a growth wafer with free-standing silicon nanowires (e.g., nanowire 11) was loaded into a thermal evaporator after growth, then nickel metal having approximately the same thickness as the silicon nanowires diameter was evaporated onto the silicon nanowires (nanowire 12). After evaporation, nickel was allowed to diffuse into the silicon nanowires by annealing at 350-550 °C (nanowire 13). Depending on the temperature of the silicon nanowires, diffusion of nickel into the silicon nanowires occurs in under 1 hour, and often under 30 minutes. For instance, if the nanowires are heating using a tube furnace, diffusion of nickel into the nanowires occurred in approximately 30 minutes. Using rapid thermal annealing (RTA) or rapid thermal processing (RTP) techniques that can reach to 350-550 °C in a few seconds, diffusion of the nickel into the nanowires occurred in about 5 minutes.

The excess nickel was then removed by etchant (TFG, Transene Co.), followed by a post-annealing period at 600 °C. All of the annealing and post-annealing steps were

carried out in hydrogen gas for 30 minutes in a tube furnace or for 5 minutes using RTP/RTA techniques (nanowire 14).

EXAMPLE 2

This example illustrates the preparation of NiSi/Si nanowire heterostructures, according to another embodiment of the invention. With reference to Fig. 3A, silicon nanowires dispersed in ethanol were deposited on a semiconductor wafer with 600 nm oxide (substrate 31 in Fig. 3A). A photolithography process was used to define nickel silicide regions as follows (see substrate 32 in Fig. 3A). Shipley S1813 photoresist was deposited by spin coating onto the wafer. The photoresist was then exposed for about 2 seconds on an ABM photoaligner using a 1 micron line-width, 2 micron pitch) striped photomask to define the nickel silicide regions. After developing for approximately 1 min, the wafer was transferred to a thermal evaporator and nickel was evaporated onto the wafer with a thickness approximately equal to the diameter of the nanowire (substrate 32). After the evaporation and lift-off of excess photoresist, annealing, etching, and post-annealing were performed using techniques similar to those described in Example 1. This method yielded NiSi/Si nanowire heterostructures with a well-defined pattern determined by the line pattern of the photomask.

EXAMPLE 3

In this example, metallic nickel silicide nanowires were formed from semiconductor silicon nanowires and characterized. The preparation of nickel silicide (NiSi) nanowires in this example uses a simple solid-state reaction between nickel and silicon nanowires under annealing conditions, similar to those discussed in Example 1.

Fig. 1B shows a typical transmission electron microscopy (TEM) image of nanowires prepared from silicon nanowires grown from 20 nm gold nanoclusters. The nanowires have substantially uniform diameters (22.8 ± 3.4 nm) with lengths of nanometers up to several micrometers. Energy dispersive X-ray spectroscopy (EDS) measurements showed that the atom ratio between nickel and silicon in the nanowires was stoichiometric (%Ni:%Si = 1.03:1). The scale bar indicates 500 nm.

Figs. 1C and 1D illustrate representative high resolution transmission electron microscopy (HRTEM) images. In these images, the scale bar represents 5 nm. These images illustrate single-crystal nickel silicide nanowire structures. Fig. 1C is a HRTEM image of a 20 nm nickel silicide nanowire prepared using silicon nanowires grown from

20 nm gold nanoclusters. The growth front of the nanowire is in the $(1\bar{1}1)$ plane. A two-dimensional Fourier transform (inset, Fig. 1C) of the TEM image of the 20 nm nanowire depicts the $[10\bar{1}]$ zone axis of the nickel silicide wire. Fig. 1D is a HRTEM image of a 32 nm nickel silicide nanowire prepared using silicon nanowires grown from 30 nm gold nanoclusters. The high yield of nickel silicide nanowires with single crystallinity extended from the controlled growth of silicon nanowire allowed additional characterization of their physical properties, as discussed below. The growth front of the nanowire is in the (001) plane. The inset of Fig. 2D shows a two-dimensional Fourier transform of the image depicting the $[2\bar{1}0]$ zone axis of the nickel silicide.

EXAMPLE 4

In this example, certain transport properties of single-crystal nickel silicide nanowires were characterized. Two-terminal and four-terminal transport measurements were performed on individual nickel silicide nanowires, fabricated using techniques similar to those described in Example 1. All of the more than 100 nanowires used in this example showed a linear I-V response and a two-probe resistance of about 1 to about 5 kOhm (kΩ). While a simple calculation using the bulk resistivity of about 10 microOhm cm (μΩ cm) for single-crystal nickel silicide nanowires gave resistances of about 80 Ohms (Ω) to about 480 Ohms for each nanowire having diameters from 20 nm to 50 nm and a conducting channel length of around 1.5 microns in these experiments, the contact resistance between the chromium/gold electrode used and the nanowires may contribute a large proportion to the total resistance measured.

As confirmation, the four-probe experiments showed that among these resistances, the true resistance of nickel silicide nanowires only accounts for less than about 50% of the measured resistance, as illustrated in Fig. 2A. This figure illustrates current vs. voltage curves of a 29 nm nickel silicide nanowire with linear responses, with curve 20 corresponding to two-terminal measurement result and curve 25 corresponding to four-terminal measurement result. In this figure, the two-probe resistance was found to be about 890 Ohm, while the true resistance of a 29 nm diameter nickel silicide nanowire was determined to be about 180 Ohm using the four-probe method, corresponding to a resistivity of about 9.2 microOhm cm (μΩ cm).

The four-probe study, performed on more than 30 nanowires with diameters of about 18 nm to about 50 nm, gave resistivities of between about 6 microOhm cm and

about 60 microOhm cm. The inset in Fig. 2A is a scanning electron microscopy (SEM) image of the 29 nm NiSi four-terminal device. The scale bar in Fig. 2A represents 1 micron. Resistivity values of larger than 10 microOhm cm were believed to be due to defects in some samples, which can be eliminated by optimizing the fabrication process, using routine techniques known to those of ordinary skill in the art. The similarity between the measured true resistivity and bulk value suggested that a diffusive transport of charge carriers is responsible and the resistivity does not rise as the sizes of our nanowires decreases.

Temperature-dependent measurements further demonstrate that the resistance of the nanowires decreases approximately linearly with temperatures from about 300 K to about 60 K, further confirming the metallic behavior of the nickel silicide nanowires.

Thus, these experiments illustrate that semiconducting silicon nanowires have been successfully transformed into metallic nickel silicide nanowires. Using previously reported carrier density value in nickel silicide the scattering mean free path was estimated to be about 5 nm, which also illustrates that further scaling down of nickel silicide nanowires to sub-10 nm dimensions could be achieved (for example, to 8 nm, 5 nm, 3 nm, or even 1 nm or less) without major changes in performance.

EXAMPLE 5

This example illustrates the transport behavior of nickel silicide nanowires under high electric field conditions by applying bias voltages of up to 2 V to the nanowires. In Fig. 2B, a maximum current of about 1.84 mA was passed through the same nanowire as in Fig. 2A (see Example 4). It was found that the nanowire broke at a bias of about 1.88 V.

Multiple experiments involving nanowire breakdowns illustrated that above a certain low bias, about 1 V in this case, all of the I-V curves observed appeared to become non-linear and showed a decrease in dI/dV (see Fig. 2B). This observation may be accounted for by additional electron-phonon scattering process. Also observed in these experiments was that nearly all of the nanowire breakdowns happened after the nonlinearity turning point. This correlation suggested that the breakdown process may be related to the elevated excitation of high energy optical phonons, and the heat dissipation it brings. SEM results (see, e.g., the inset in Fig. 2B) showed that the nanowire was broken in approximately its middle, which would have a peak temperature caused by dissipative self-heating. The scale bar represents 500 nm in Fig. 2B. This observation

also suggested that the breakdown mechanism may be due to high temperature melting effect.

Using the I-V and diameter data in Fig. 2, the maximum current density, J_{max}, was determined to be about 3×10^8 A/cm^2 for these particular nanowires. However, some nanowires were found to have lost contact with the metal electrodes after high bias, but remained intact after reaching maximum currents as high as 5 mA, suggesting that the current carrying capability can be even higher for certain single-crystal nickel silicide nanowires under optimized conditions, for example, as high as about 10 mA or about 15 mA, or even higher. Moreover, the total amount of current can be scaled up by using NiSi nanowires with larger diameters.

Thus, in summary, the existence of such a high current density may be attributable to the single crystallinity of the nanowires studied. The localized energy dissipation at grain boundary and defect sites would be largely quenched. Also, the absence of grain boundaries suppressed void diffusion paths, thereby resulting in high resistance to electromigration until under extremely high fields.

EXAMPLE 6

In this example, the integration of metallic nickel silicide nanowires into nanoscale devices made by semiconducting silicon nanowires was illustrated. NiSi/Si nanowire heterostructures were fabricated via lithographically defined nickel silicide regions on silicon nanowires, using techniques similar to those discussed in Example 2. In this example, a periodic mask was used to produce a periodic heterostructure in the final nanowire; however, other patterns (including nonperiodic ones) may also be created.

Fig. 3B is a dark field optical image of a single NiSi/Si heterostructured nanowire. The lighter segments 35 correspond to silicon and the dark segments 36 to nickel silicide. The difference in contrast may be attributable to the different reflectivities of the two materials. Control experiments (not shown) using pure silicon nanowires or pure nickel nanowires also showed the same general contrast difference using optical microscopy. The periodic heterostructure extended up to several tens of micrometers over the full length of the nanowire. The scale bar in Fig. 3B is 40 microns.

A typical TEM image of a NiSi/Si heterostructured nanowire is shown in Fig. 3C. The bright segments of the nanowire (average length of about 0.93 microns) corresponded to silicon, while dark segments (average length of about 1.03 microns)

corresponded to nickel silicide. This contrast difference is believed to be due to a larger electron scattering cross section in nickel than in silicon This modulation in axial composition was also confirmed by EDS analysis. The scale bar represents 1 micron.

A HRTEM image of the junction between nickel silicide and silicon (Fig. 3D) showed an atomically abrupt interface. The insets in Fig. 3D illustrate two-dimensional Fourier transforms of the image depicting the [110] and [111] zone axes of NiSi and Si, respectively, with a nickel silicon growth front in the (221) plane and Si growth front in the (112) plane. The scale bar indicates 5 nm.

EXAMPLE 7

In this example, the transport properties of certain NiSi/Si heterostructured nanowires were studied. Field-effect transistor (FET) devices were fabricated using NiSi/p-Si/NiSi nanowire heterostructures similar to those described in Example 6. The source and drain contact regions were fabricated on nickel silicide domains far from the doped silicon channel. Fig. 4A presents typical FET characteristics of such a heterojunction. The linear source-drain current (I_{SD}) vs. bias voltage (V_{SD}) curves suggested that the NiSi/Si contact is approximately ohmic at room temperature, and the changes in I_{SD} at different back-gate voltages (V_G) demonstrated that the p-silicon region functioned as a switching channel. A gate sweep (I_{SD} vs. V_G, inset, Fig. 4A) obtained from the same device at a saturation bias voltage of about -3 V showed that the holes can be depleted at a threshold voltage of about 3.4 V.

Scanning gate microscopy (SGM) images showed reduced conductance at +9 V gate voltage (Fig. 4C) and enhanced conductance at –9 V gate voltage (Fig. 4D) on the atomic force microscopy (AFM) tip. This region is generally confined to the silicon part of the nanowire heterostructure when compared with scanning electron microscopy (SEM) image (Fig. 4B) and dark field optical image (Inset, Fig. 4B). This illustrates that this is a spatially well-defined metal-semiconductor system. The scale bar in both images is 3 microns.

Temperature-dependent transport measurement on a single NiSi/p-Si junction were also performed. It was determined that the effective Shottky barrier height (Φ_B) for holes was about 640 meV, suggesting that the ohmic contacts between nickel silicide and silicon may be due to a "squeezing out" of the dopant atoms toward the interface during formation of nickel silicide thereby forming a highly doped silicon region at the

interface, which reduces the barrier width and promotes direct tunneling current. The scale bars in Fig. 4C and 4D each represent 3 microns.

EXAMPLE 8

This example illustrates the preparation of certain NiSi/Si nanowire heterostructures, according to another embodiment of the invention.

Si nanowires dispersed in ethanol were deposited on a Si wafer with 600 nm thermal oxide, and then the substrate was coated with photoresist (Shipley 1813, Rohm and Haas Electronics Materials LLC, North Andover, MA). The photoresist was exposed for about 2 s on an ABM photoaligner using a simple striped pattern with a 2 micrometer pitch: 1 micrometer line-width and 1 micrometer spacing. After developing for about 1 min, the wafer was transferred to a thermal evaporator and Ni was evaporated with a thickness equal to the average nanowire diameter. Following lift-off, the samples were annealed and etched. Ultrasmall NiSi/Si/NiSi nanowire heterostructures were fabricated using crossed Si/SiO_2 core-shell nanowires using established protocols (see, e.g., Serial No. 10/152,490, entitled, "Nanoscale Wires and Related Devices," filed May 20, 2002) as masks to define the lengths of the unreacted Si regions. The crossed nanowire structures were assembled on Si_3N_4 8 membrane window grids (Structure Probe Inc., West Chester, PA) by fluidic assembly (see, e.g., Serial No. 10/152,490, entitled, "Nanoscale Wires and Related Devices," filed May 20, 2002), and then Ni was evaporated and annealed. The Si/SiO_2 core-shell nanowires were removed with hydrogen fluoride solution (Transene Co., Danvers, MA) to enable direct TEM imaging of the NiSi/Si/NiSi heterostructure on the Si_3N_4 membranes.

Fig. 6A is a schematic illustrating the production of NiSi/Si/NiSi heterostructures. In this figure, on surface 61, Si nanowires 63 are crossed with 3 Si/SiO_2 core/shell nanowires 65. Deposition, annealing and removal of excess Ni yields NiSi regions 67 separated by Si in the nanowire (masked by nanowires 65), as seen on surface 62.

Fig. 6B is a TEM image of a NiSi/Si/NiSi nanowire heterostructure, following removal of the crossed nanowire mask, showing a well-defined silicon channel of 20 nm in this 10 nm diameter NiSi/Si/NiSi heterostructure. The dark regions 68 correspond to NiSi and the light regions 69 to Si, with NiSi/Si interfaces 64 highlighted by black arrows. The scale bar represents 10 nm. The inset shows a TEM image of the same nanowire before silicidation. The crossed Si/SiO_2 core/shell nanowire 66 (approximately

vertical in image) was used as a mask to define the Si region and removed after silicidation. The scale bar in the inset represents 20 nm. The sample was prepared and imaged on a 50 nm thick Si_3N_4 membrane. Additionally, a cross-sectional measurement of the nanowire, as shown in Fig. 6C, shows a relatively sharp boundary between the Si portions and the NiSi portions of the heterostructure.

Figs. 6D-6F shows additional examples, in which Si/SiO_2 core/shell nanowire having other diameters were used as nanowire masks. Fig. 6D shows a Si/SiO_2 core/shell nanowire having a diameter of 148.1 ± 9.4 nm (left) that was used to produce a silicon channel of 134.5 ± 15.8 nm in a NiSi/Si/NiSi heterostructure (right). Similarly, Fig. 6E shows a Si/SiO_2 core/shell nanowire having a diameter of 50.0 ± 3.1 nm (left) used to produce a silicon channel of 38.0 ± 7.3 nm (right), and Fig. 6F shows a Si/SiO_2 core/shell nanowire having a diameter of 19.8 ± 2.0 nm (left) used to produce a silicon channel of about 10 nm (right).

The TEM results indicate lateral diffusion of several nanometers during the formation of NiSi, and shows that it is possible to prepare shorter channel devices in a well-defined manner by varying the diameter of the nanowire mask. More generally, the capability of transforming Si to NiSi in a spatially well-defined manner to form NiSi/Si nanowire heterostructures and superlattices with atomically sharp metal/semiconductor interfaces, opens up the ability of integrating both active devices and high-performance interconnects from a single nanoscale building block. By extending this approach to crossed nanowires, it is possible to assemble large and dense arrays, for example using Langmuir-Blodgett assembly techniques, of transistors and other devices, for example, for use in hybrid integrated circuits, stand-alone integrated nanosystems, or the like.

Of course, the technique illustrated in Figs. 6A and 6B can be applied to any of the embodiments described herein involving introducing one species into another species, such as diffusing at least a portion of a bulk metal into a semiconductor wire.

EXAMPLE 9

This example illustrates the correlation between structure and transport, in various NiSi/Si/NiSi heterostructures, prepared using techniques similar to those described above.

Fig. 7C illustrates current versus voltage, for nickel-contacting silicon nanowires (non-annealed). These wires are shown in Figs. 7A and 7B. Fig. 7D illustrates the formation of a single crystal silicide from a silicon nanowire, at 350 °C, annealed for 5

minutes. Figs. 7E-7G illustrate performance of the Si/NiSi heterostructure after annealing of the nickel to the silicon nanowire to form NiSi. Scale bars in Figs. 7A and 7E represent 1 micron; scale bars in Figs. 7B, 7D, and 7F represent 50 nm.

While several embodiments of the present invention have been described and illustrated herein, those of ordinary skill in the art will readily envision a variety of other means and/or structures for performing the functions and/or obtaining the results and/or one or more of the advantages described herein, and each of such variations and/or modifications is deemed to be within the scope of the present invention. More generally, those skilled in the art will readily appreciate that all parameters, dimensions, materials, and configurations described herein are meant to be exemplary and that the actual parameters, dimensions, materials, and/or configurations will depend upon the specific application or applications for which the teachings of the present invention is/are used. Those skilled in the art will recognize, or be able to ascertain using no more than routine experimentation, many equivalents to the specific embodiments of the invention described herein. It is, therefore, to be understood that the foregoing embodiments are presented by way of example only and that, within the scope of the appended claims and equivalents thereto, the invention may be practiced otherwise than as specifically described and claimed. The present invention is directed to each individual feature, system, article, material, kit, and/or method described herein. In addition, any combination of two or more such features, systems, articles, materials, kits, and/or methods, if such features, systems, articles, materials, kits, and/or methods are not mutually inconsistent, is included within the scope of the present invention.

All definitions, as defined and used herein, should be understood to control over dictionary definitions, definitions in documents incorporated by reference, and/or ordinary meanings of the defined terms.

The phrase "and/or," as used herein in the specification and in the claims, should be understood to mean "either or both" of the elements so conjoined, i.e., elements that are conjunctively present in some cases and disjunctively present in other cases. Other elements may optionally be present other than the elements specifically identified by the "and/or" clause, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, a reference to "A and/or B", when used in conjunction with open-ended language such as "comprising" can refer, in one embodiment, to A only

(optionally including elements other than B); in another embodiment, to B only (optionally including elements other than A); in yet another embodiment, to both A and B (optionally including other elements); etc.

As used herein in the specification and in the claims, the phrase "at least one," in reference to a list of one or more elements, should be understood to mean at least one element selected from any one or more of the elements in the list of elements, but not necessarily including at least one of each and every element specifically listed within the list of elements and not excluding any combinations of elements in the list of elements. This definition also allows that elements may optionally be present other than the elements specifically identified within the list of elements to which the phrase "at least one" refers, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, "at least one of A and B" (or, equivalently, "at least one of A or B," or, equivalently "at least one of A and/or B") can refer, in one embodiment, to at least one, optionally including more than one, A, with no B present (and optionally including elements other than B); in another embodiment, to at least one, optionally including more than one, B, with no A present (and optionally including elements other than A); in yet another embodiment, to at least one, optionally including more than one, A, and at least one, optionally including more than one, B (and optionally including other elements); etc.

It should also be understood that, unless clearly indicated to the contrary, in any methods claimed herein that include more than one act, the order of the acts of the method is not necessarily limited to the order in which the acts of the method are recited.

In the claims, as well as in the specification above, all transitional phrases such as "comprising," "including," "carrying," "having," "containing," "involving," "holding," and the like are to be understood to be open-ended, i.e., to mean including but not limited to. Only the transitional phrases "consisting of" and "consisting essentially of" shall be closed or semi-closed transitional phrases, respectively, as set forth in the United States Patent Office Manual of Patent Examining Procedures, Section 2111.03.

What is claimed is:

CLAIMS

1. A method, comprising:

providing a bulk metal adjacent a semiconductor wire; and

diffusing at least a portion of the bulk metal into at least a portion of the semiconductor wire, the semiconductor wire comprising at least one portion having a smallest dimension of less than about 500 nm.

2. The method of claim 1, wherein the bulk metal comprises a transition metal.

3. The method of claim 2, wherein the transition metal includes at least one of a Group IIIB element, a Group IVB element, a Group VB element, a Group VIB element, a Group VIIB element, and a Group VIIIB element.

4. The method of claim 3, wherein the bulk metal comprises a Group VIIIB element.

5. The method of claim 1, wherein the bulk metal comprises nickel.

6. The method of claim 1, wherein the bulk metal consists essentially of nickel.

7. The method of claim 1, wherein the semiconductor comprises an elemental semiconductor.

8. The method of claim 7, wherein the elemental semiconductor comprises at least one of silicon, gallium, germanium, carbon, tin, selenium, tellurium, boron, or phosphorous.

9. The method of claim 7, wherein the elemental semiconductor comprises a Group IV semiconductor.

10. The method of claim 7, wherein the elemental semiconductor comprises Si.

11. The method of claim 7, wherein the elemental semiconductor consists essentially of Si.

12. The method of claim 1, wherein the smallest dimension is less than 200 nm.

13. The method of claim 1, wherein the smallest dimension is less than 150 nm.

14. The method of claim 1, wherein the smallest dimension is less than 100 nm.

15. The method of claim 1, wherein the smallest dimension is less than 80 nm.

16. The method of claim 1, wherein the smallest dimension is less than 70 nm.

17. The method of claim 1, wherein the smallest dimension is less than 60 nm.

18. The method of claim 1, wherein the smallest dimension is less than 40 nm.

19. The method of claim 1, wherein the smallest dimension is less than 20 nm.

20. The method of claim 1, wherein the smallest dimension is less than 10 nm.

21. The method of claim 1, wherein the smallest dimension is less than 5 nm.

22. The method of claim 1, wherein the wire has an aspect ratio of at least 4:1.

23. The method of claim 1, wherein the wire has an aspect ratio of at least 10:1.

24. The method of claim 1, wherein the wire has an aspect ratio of at least 100:1.

25. The method of claim 1, wherein the wire has an aspect ratio of at least 1000:1.

26. The method of claim 1, wherein the wire is a single crystal.

27. An article, comprising:

a wire comprising at least one metal silicide, the wire being a single crystal.

28. The article of claim 27, wherein the metal comprises a transition metal.

29. The article of claim 28, wherein the transition metal includes at least one of a Group IIIB element, a Group IVB element, a Group VB element, a Group VIB element, a Group VIIB element, and a Group VIIIB element.

30. The article of claim 29, wherein the metal is a Group VIIIB element.

31. The article of claim 30, wherein the metal comprises nickel.

32. The article of claim 27, wherein the wire comprises at least one portion having a smallest dimension of less than about 500 nm.

33. The article of claim 27, wherein the wire has an aspect ratio of at least 4:1.

34. The article of claim 27, wherein the wire is part of a device.

35. The article of claim 34, wherein the device is an electronic device.

36. The article of claim 34, wherein the device is a switch.

37. The article of claim 34, wherein the device is a logic unit.

38. The article of claim 34, wherein the device is a transistor.

39. The article of claim 38, wherein the transistor is a field effect transistor.

40. The article of claim 34, wherein the device comprises a digital circuit.

41. The article of claim 27, wherein the metal silicide comprises a stoichiometric ratio of silicon and at least one metal.

42. The article of claim 27, wherein the wire has a resistivity of less than about 60 microOhm cm.

43. The article of claim 27, wherein the wire is able to carry a current density of at least about 10^8 A/cm^2.

44. An article, comprising:

a wire comprising a compound having a stoichiometric ratio of silicon and at least one metal, the wire comprising at least one portion having a smallest dimension of less than about 500 nm.

45. The article of claim 44, wherein the metal comprises a transition metal.

46. The article of claim 45, wherein the transition metal comprises nickel.

47. The article of claim 44, wherein the wire comprises at least one portion having a smallest dimension of less than about 500 nm.

48. The article of claim 44, wherein the wire has an aspect ratio of at least 4:1.

49. The article of claim 44, wherein the wire is part of a device.

50. The article of claim 44, wherein the wire is a single crystal.

51. The article of claim 44, wherein the wire has a resistivity of less than about 60 microOhm cm.

52. The article of claim 44, wherein the wire is able to carry a current density of at least about 10^8 A/cm^2.

53. The article of claim 44, wherein the wire comprises two regions differing in composition, at least one of the two regions comprising the compound having the stoichiometric ratio of silicon and at least one metal.

54. An article, comprising:

a wire comprising at least one metal silicide, the wire having a resistivity of less than about 60 microOhm cm.

55. The article of claim 54, wherein the metal comprises a transition metal.

56. The article of claim 55, wherein the metal comprises nickel.

57. The article of claim 54, wherein the wire comprises at least one portion having a smallest dimension of less than about 500 nm.

58. The article of claim 54, wherein the wire has an aspect ratio of at least 4:1.

59. The article of claim 54, wherein the wire is part of a device.

60. The article of claim 54, wherein the wire is a single crystal.

61. The article of claim 54, wherein the metal silicide comprises a stoichiometric ratio of silicon and at least one metal.

62. The article of claim 54, wherein the wire is able to carry a current density of at least about 10^8 A/cm^2.

63. The article of claim 54, wherein the wire comprises two regions differing in composition, at least one of the two regions comprising the metal silicide.

64. An article, comprising:

a wire comprising at least one metal silicide, the wire being able to carry a current density of at least about 10^8 A/cm^2.

65. The article of claim 64, wherein the metal comprises a transition metal.

66. The article of claim 65, wherein the metal comprises nickel.

67. The article of claim 64, wherein the wire comprises at least one portion having a smallest dimension of less than about 500 nm.

68. The article of claim 64, wherein the wire has an aspect ratio of at least 4:1.

69. The article of claim 64, wherein the wire is part of a device.

70. The article of claim 64, wherein the wire is a single crystal.

71. The article of claim 64, wherein the metal silicide comprises a stoichiometric ratio of silicon and at least one metal.

72. The article of claim 64, wherein the wire has a resistivity of less than about 60 microOhm cm.

73. The article of claim 64, wherein the wire comprises two regions differing in composition, at least one of the two regions comprising the metal silicide.

74. An article, comprising:

a wire comprising at least two regions differing in composition, at least one region comprising a metal silicide, the wire comprising at least one portion having a smallest dimension of less than about 500 nm.

75. The article of claim 74, wherein the metal comprises a transition metal.

76. The article of claim 75, wherein the metal comprises nickel.

77. The article of claim 74, wherein the wire has an aspect ratio of at least 4:1.

78. The article of claim 74, wherein the wire is part of a device.

79. The article of claim 74, wherein the metal silicide comprises a stoichiometric ratio of silicon and at least one metal.

80. The article of claim 74, wherein the wire has a resistivity of less than about 60 microohm cm.

81. The article of claim 74, wherein the wire is able to carry a current density of at least about 10^8 A/cm^2.

82. The article of claim 74, wherein each of the at least two regions independently comprises a metal silicide.

83. The article of claim 74, wherein two of the at least two regions define a boundary therebetween, the boundary being atomically abrupt.

84. The article of claim 74, the at least two regions comprising a first region having a composition and a second region having a composition different from the first region, the first region and the second region overlapping to form an overlap region having a composition that is a mixture of the compositions of the first and second regions, wherein the composition of the overlap region comprises between about 10 vol% and about 90 vol% of the composition of the first region with a complementary amount of the composition of the second region.

85. An article, comprising:

a wire comprising at least two regions differing in composition and a boundary between the at least two regions, the boundary having a maximum dimension of less than about 500 nm, wherein at least one region comprises a metal silicide.

86. The article of claim 85, wherein the metal comprises a transition metal.

87. The article of claim 86, wherein the metal comprises nickel.

88. The article of claim 85, wherein the wire has an aspect ratio of at least 4:1.

89. The article of claim 85, wherein the wire is part of a device.

90. The article of claim 85, wherein the metal silicide comprises a stoichiometric ratio of silicon and at least one metal.

91. The article of claim 85, wherein the wire has a resistivity of less than about 60 microOhm cm.

92. The article of claim 85, wherein the wire is able to carry a current density of at least about 10^8 A/cm^2.

93. The article of claim 85, wherein the maximum dimension is less than 200 nm.

94. The article of claim 85, wherein the boundary is an atomically abrupt boundary.

95. The article of claim 85, wherein the at least two regions each independently comprises a metal silicide.

96. A method, comprising:

diffusing a material into at least a portion of a wire, the wire comprising at least one portion having a smallest dimension of less than about 500 nm.

97. The method of claim 96, wherein the material comprises a metal.

98. The method of claim 97, wherein the metal comprises nickel.

99. The method of claim 96, wherein the wire comprises a semiconductor.

100. The method of claim 99, wherein the semiconductor comprises silicon.

101. The method of claim 96, comprising diffusing the first material into a first portion of a wire without diffusing the first material into a second portion of the wire.

102. The method of claim 101, wherein the first portion and the second portion of the wire are defined by a mask positioned proximate the wire.

103. The method of claim 102, wherein the mask comprises photoresist.

104. The method of claim 102, wherein the mask comprises a nanoscale wire.

105. The method of claim 104, wherein the nanoscale wire comprises a core and a shell.

106. The method of claim 104, further comprising positioning a mask proximate the semiconductor, the mask defining, at least in part, the portion of the semiconductor that at least a portion of the bulk metal diffuses into.

107. The method of claim 106, wherein the mask comprises photoresist.

108. The method of claim 106, wherein the mask comprises a nanoscale wire.

109. The method of claim 108, wherein the nanoscale wire comprises a core and a shell.

110. A method, comprising:

diffusing a metal into at least a portion of a semiconductor nanoscale wire to form a stoichiometric ratio of metal atoms to semiconductor atoms within the portion of the semiconductor nanoscale wire.

111. The method of claim 110, wherein the metal comprises a transition metal.

112. The method of claim 110, wherein the metal comprises nickel.

113. The method of claim 110, wherein the metal consists essentially of nickel.

114. The method of claim 110, wherein the semiconductor comprises an elemental semiconductor.

115. The method of claim 110, wherein the elemental semiconductor comprises Si.

116. The method of claim 110, wherein the elemental semiconductor consists essentially of Si.

117. A method, comprising:

bulk-doping at least a portion of a nanoscale wire after growth of the nanoscale wire.

118. The method of claim 117, wherein bulk-doping comprises doping a center portion of the nanoscale wire.

119. The method of claim 117, comprising bulk-doping the nanoscale wire to increase the conductivity of the nanoscale wire.

120. The method of claim 117, comprising diffusing a metal into at least a portion of the semiconductor nanoscale wire.

121. A method, comprising:

diffusing a material into a center portion of a semiconductor wire, the semiconductor wire comprising at least one portion having a smallest dimension of less than about 500 nm.

122. The method of claim 121, comprising diffusing at least a portion of the material to alter the conductivity of the portion of the semiconductor wire.

123. The method of claim 121, wherein the material comprises a metal.

124. The method of claim 123, wherein the metal comprises a transition metal.

5

125. The method of claim 123, wherein the metal comprises nickel.

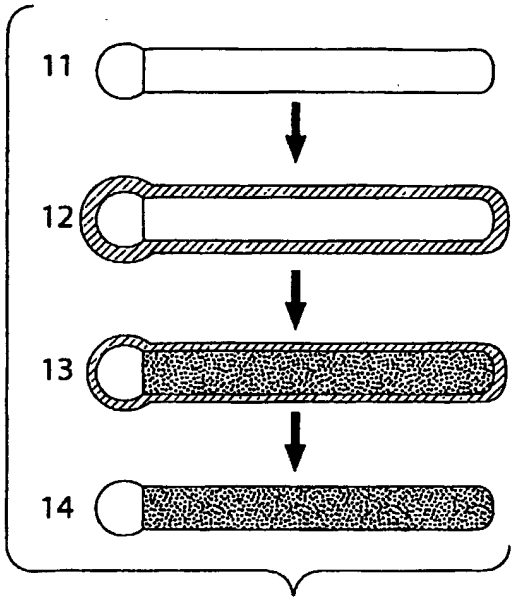


Fig. 1A

Fig. 1B

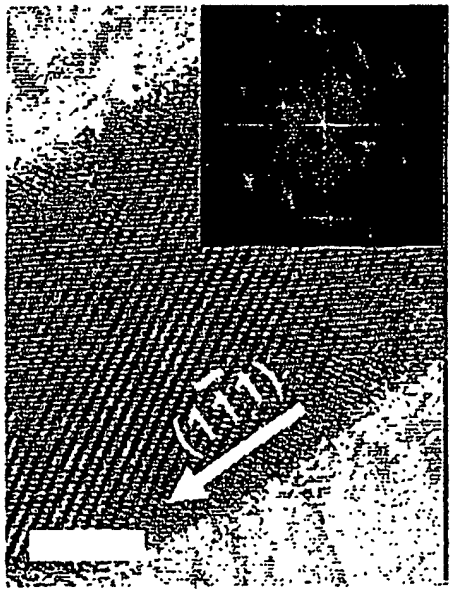


Fig. 1C

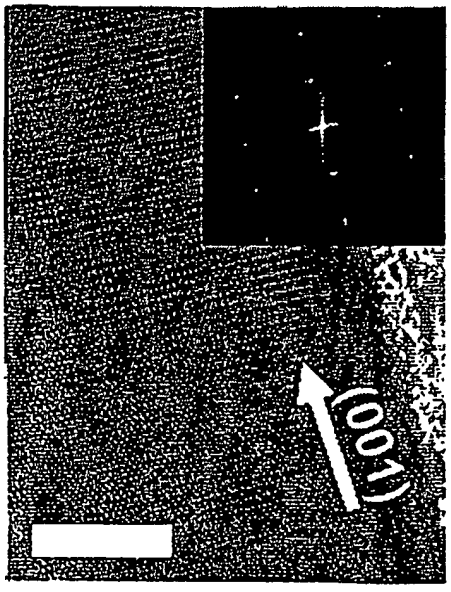


Fig. 1D

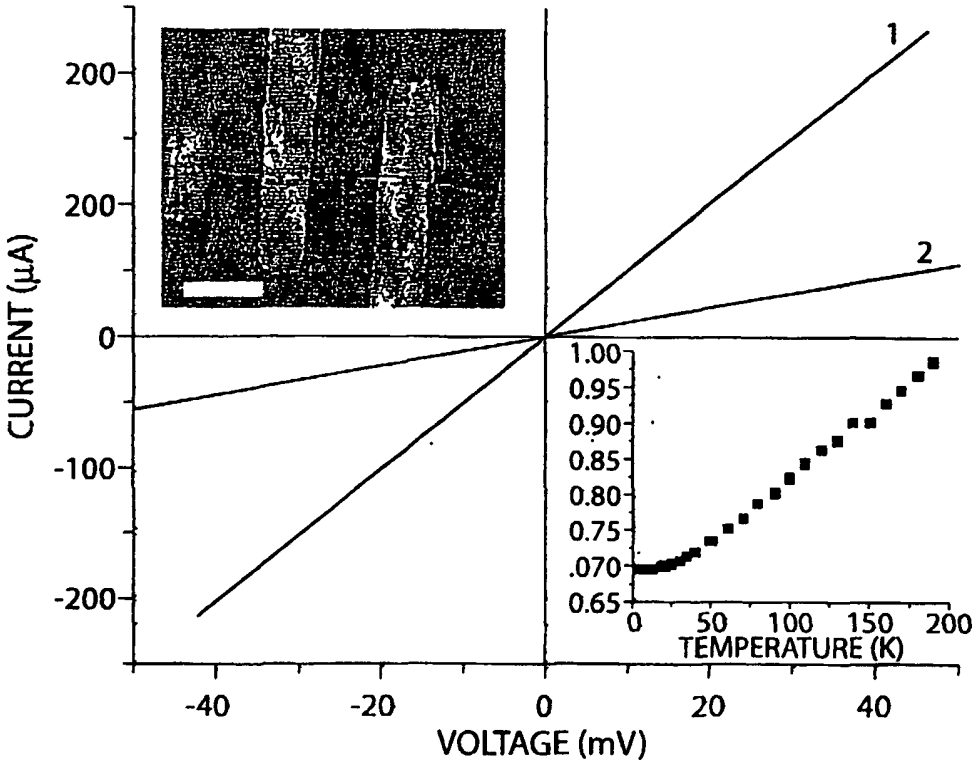

CURRENT (μA)
200
200
0
-100
-200
-40
-20
0
20
40
VOLTAGE (mV)
1
2
1.00
0.95
0.90
0.85
0.80
0.75
.070
0.65
0
50
100
150
200
TEMPERATURE (K)

Fig. 2A

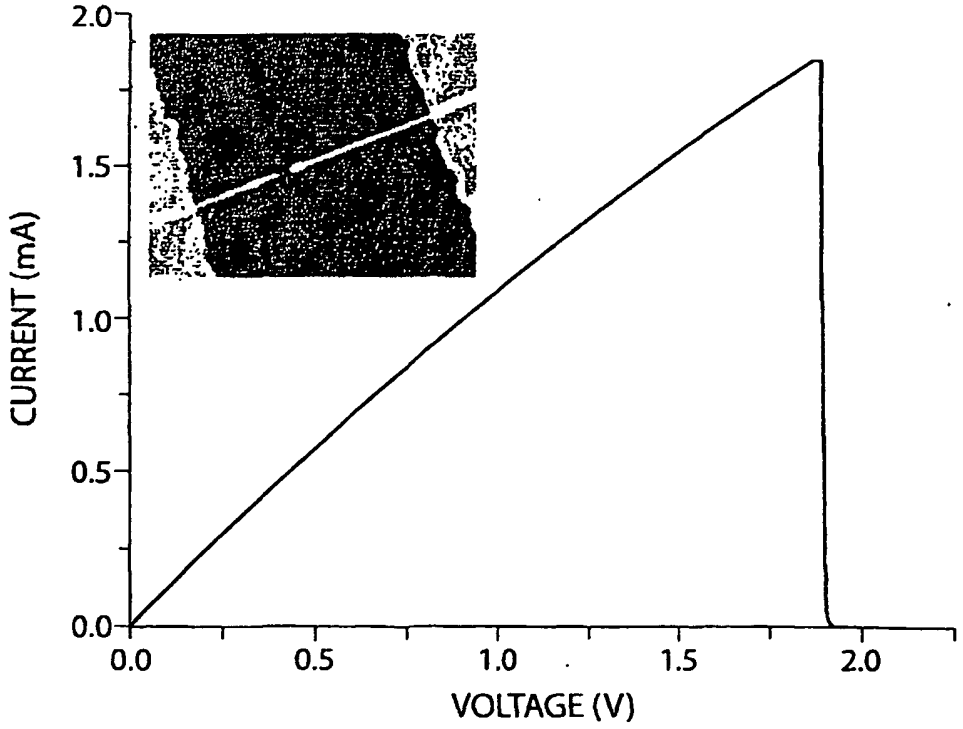

CURRENT (mA)
2.0
1.5
1.0
0.5
0.0
0.0
0.5
1.0
1.5
2.0
VOLTAGE (V)

Fig. 2B

Fig. 3A

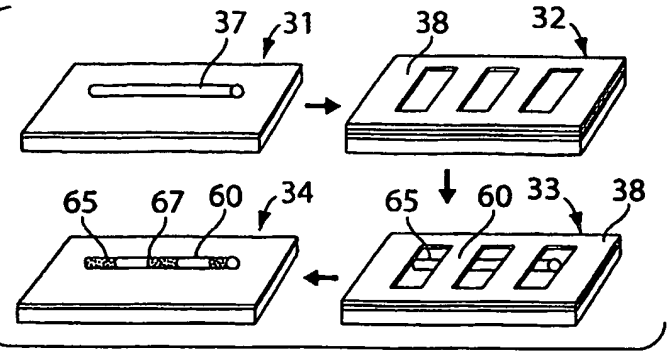


Fig. 3B

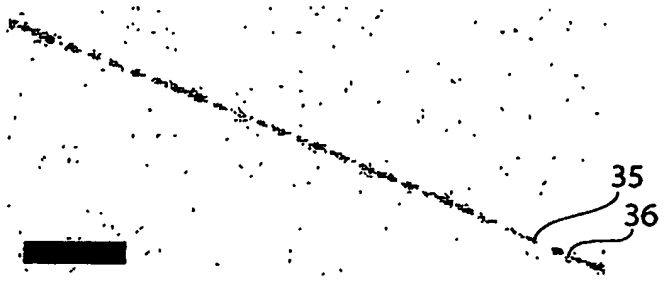


Fig. 3C

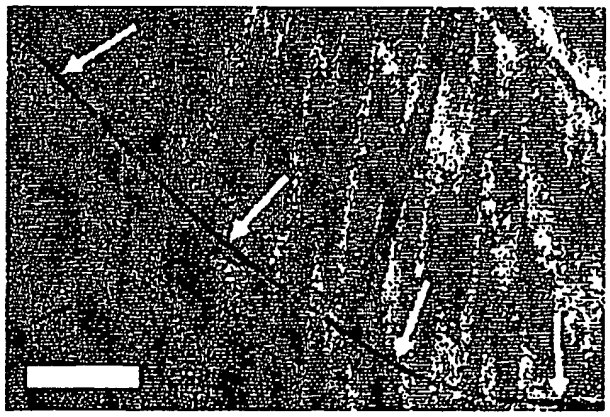
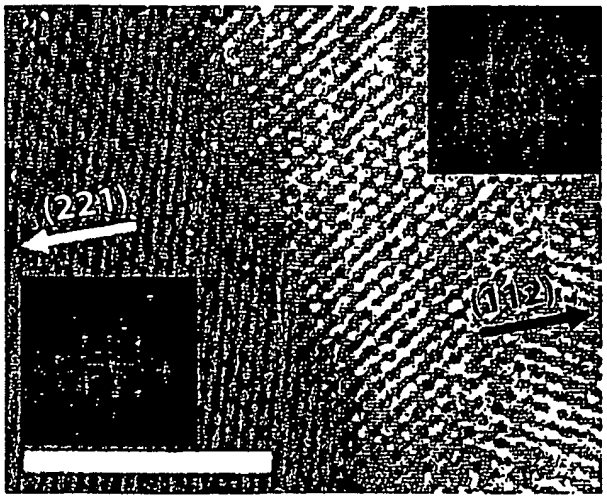


Fig. 3D



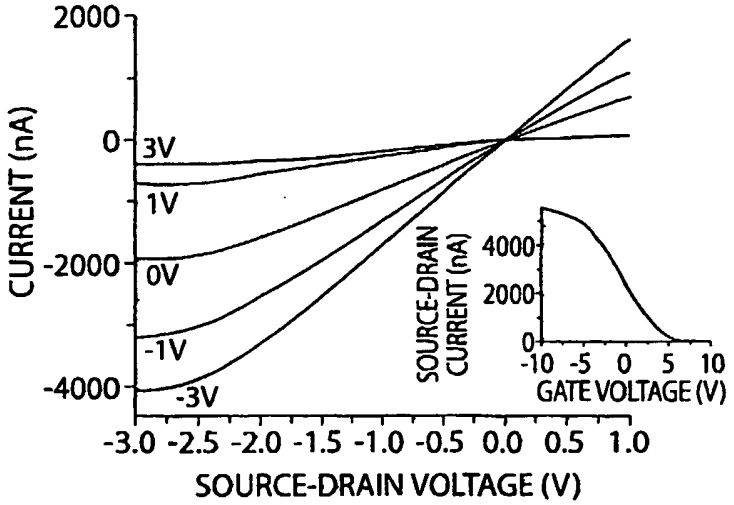


Fig. 4A

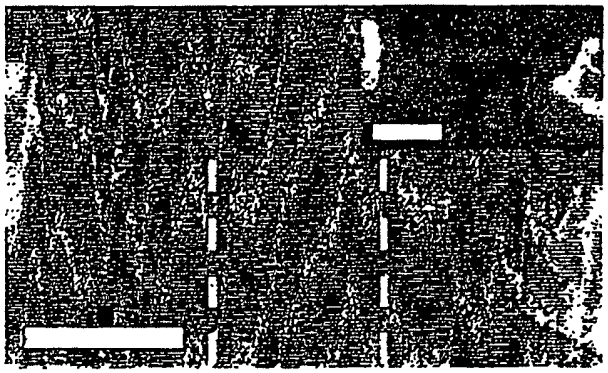


Fig. 4B

Fig. 4C

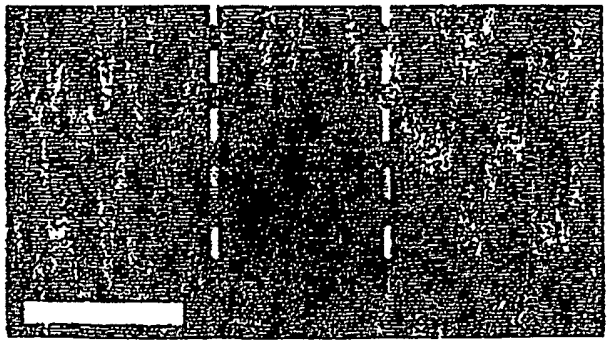


Fig. 4D

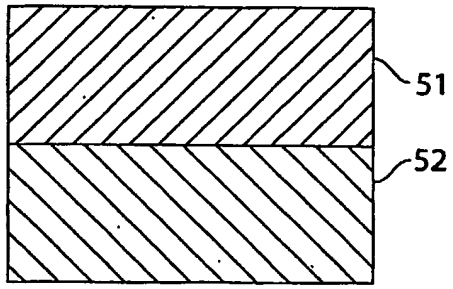


Fig. 5A

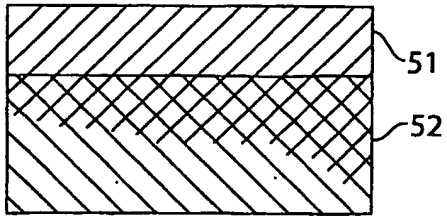


Fig. 5B

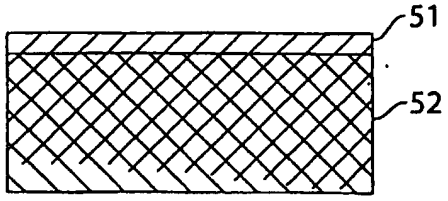


Fig. 5C

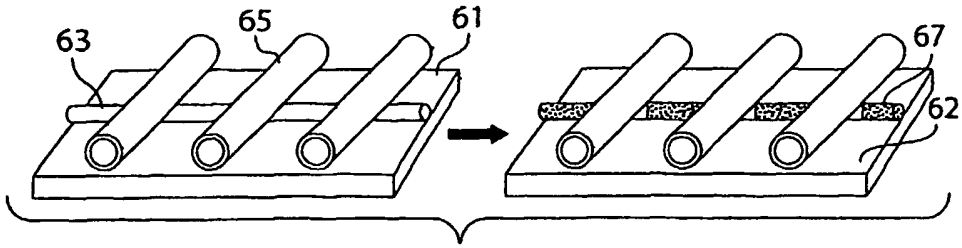


Fig. 6A

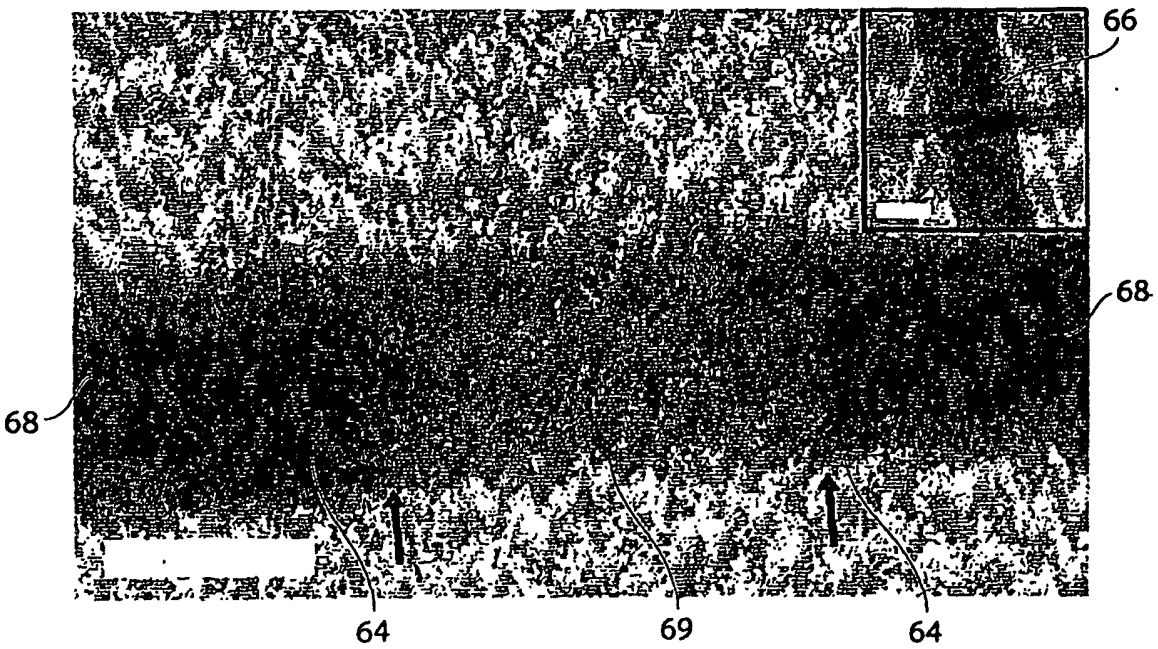


Fig. 6B

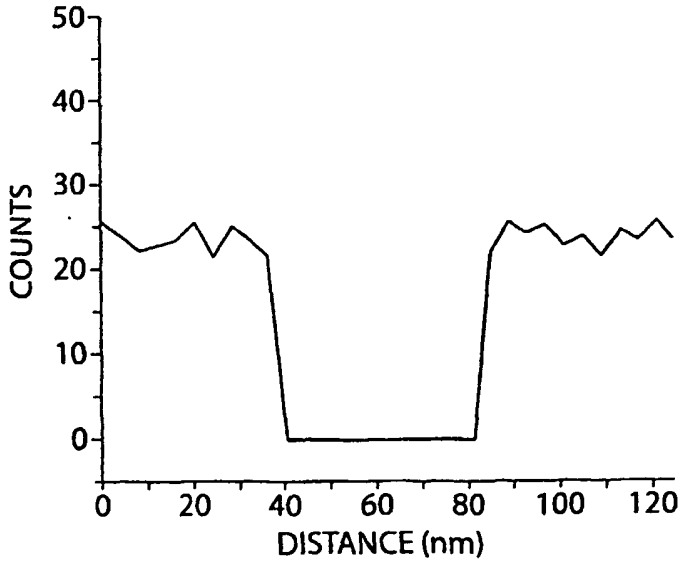


Fig. 6C

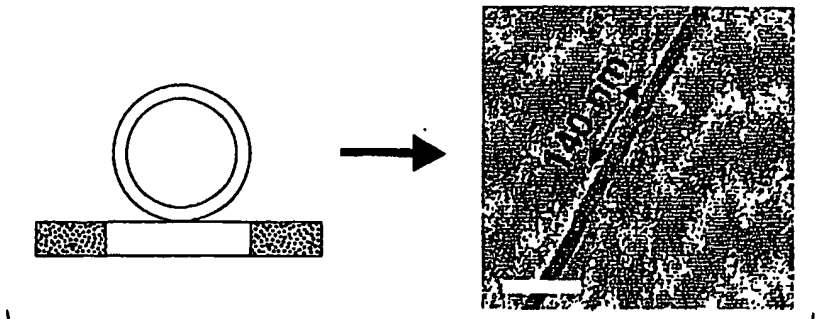


Fig. 6D

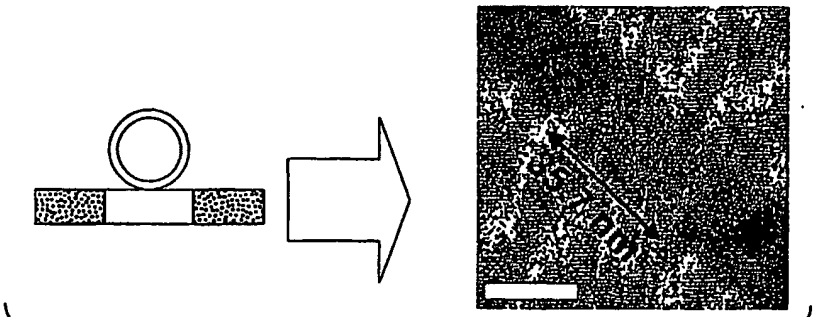


Fig. 6E

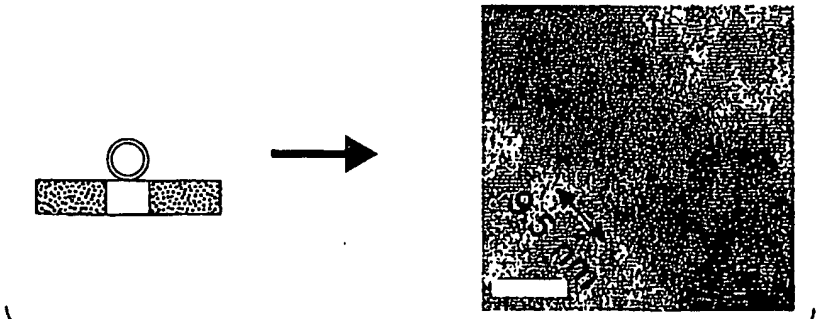


Fig. 6F

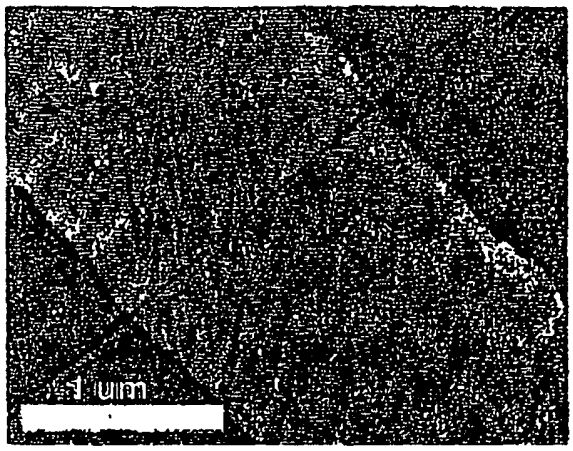


Fig. 7A

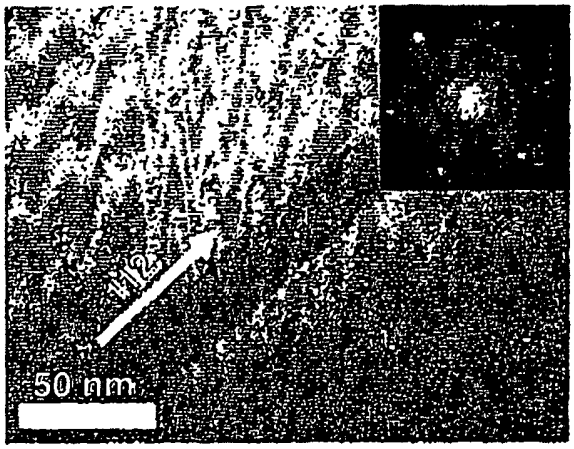


Fig. 7B

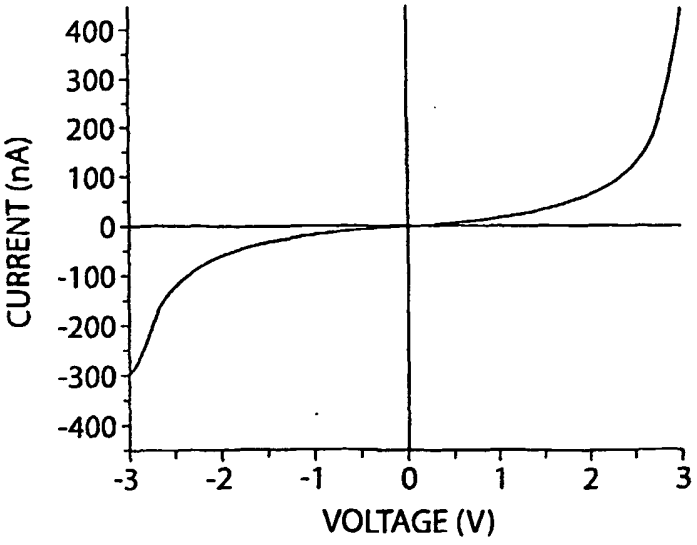


Fig. 7C

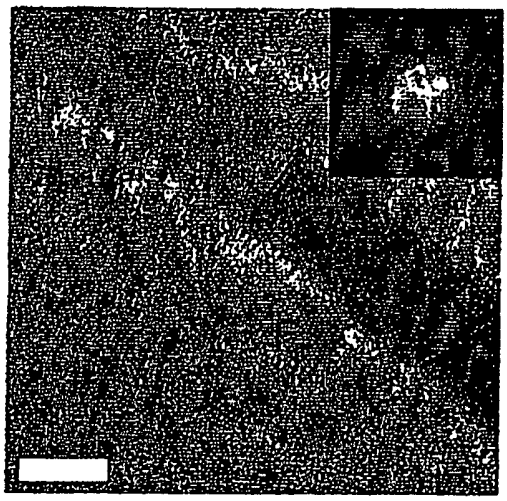


Fig. 7D

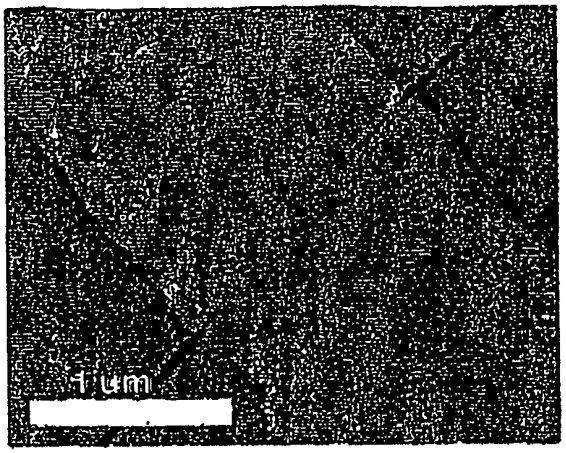


Fig. 7E

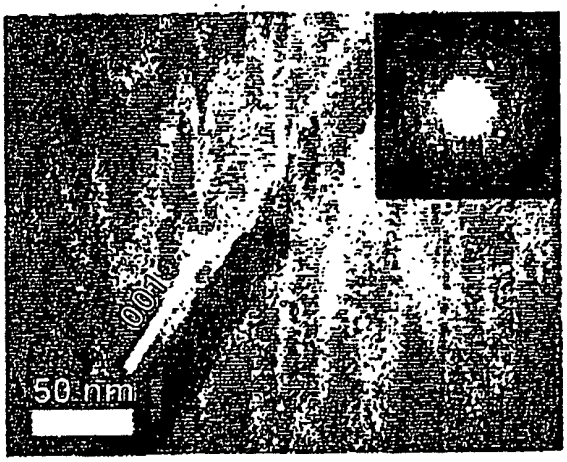


Fig. 7F

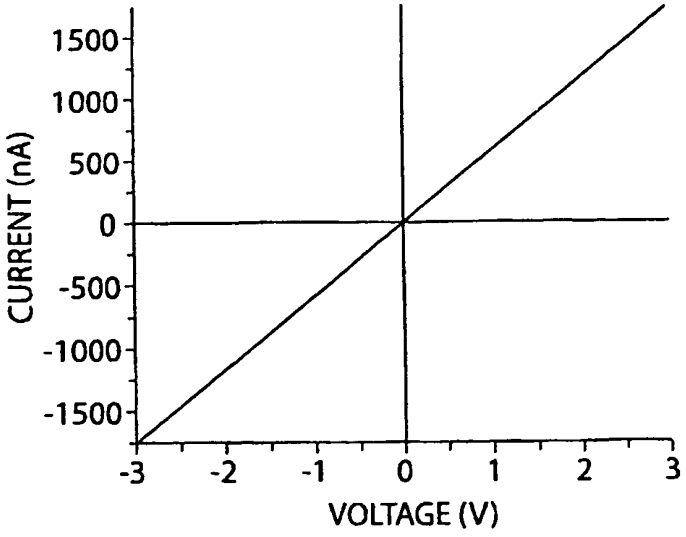


Fig. 7G